

MODEL NAME : *BBV00/BBV10*  
PCB NO : *LA-D993P*

BOM P/N :

# Dell/Compal Confidential

## Schematic Document

### KABYLAKE-H

2016-11-01

Rev: 1.0 (A00)

@ : Nopop Component

CONN@ : Connector Component

R1@ / R3@ : R1/R3 CPN for CPU, GPU, PCB

EMC@ : Pop of EMI parts

S4G@ : Samsung GDDR5 4G for GPU

M4G@ : Micron GDDR5 4G for GPU

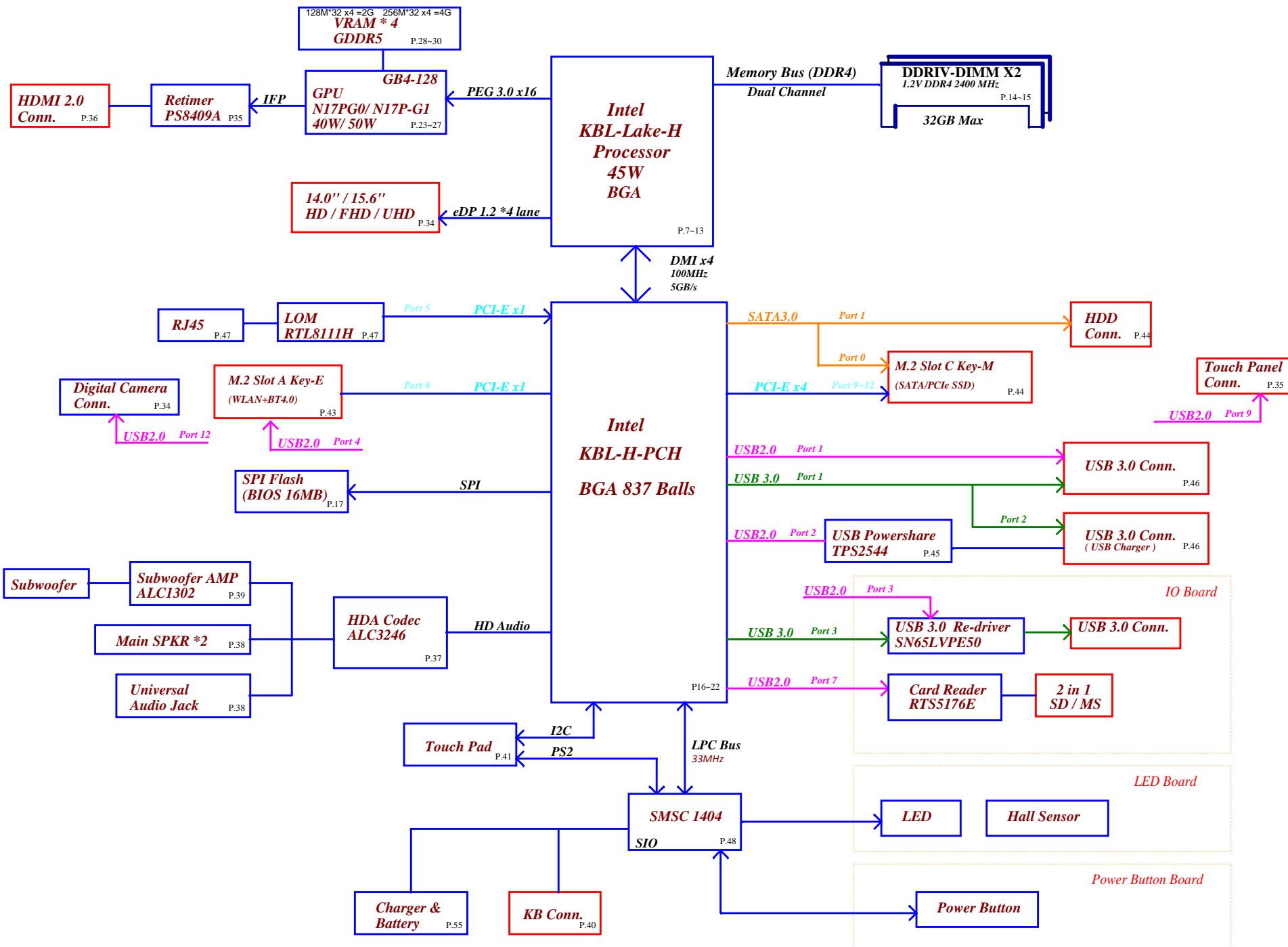
H4G@ : Hynix GDDR5 4G for GPU

BreakDown@ : For measure power consumption

14G0@ : 14" N17P-G0

15G1@ : 15" N17P-G1

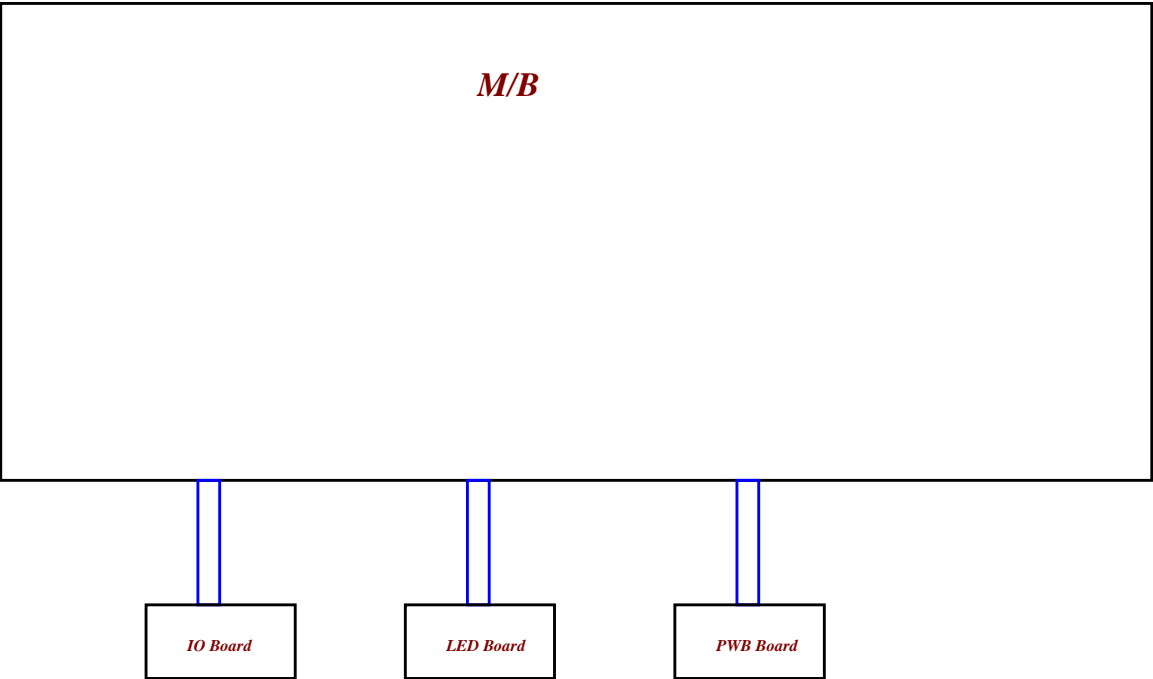
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File Name :



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Board ID	Resistor
X00	N/A
X01	
X02	
X03	
X04	22.1K
A00	

USB3	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	None
5	None
6	None

USB 2.0	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	NGFF-1 WLAN + BT
5	None
6	None
7	None
8	None
9	Touch screen
10	None
11	None
12	CAMERA

DDI	DESTINATION
1	Alpine Ridge
2	Alpine Ridge
3	None

LPC	DESTINATION
LPC0	MEC5085
LPC1	DEBUG PORT

PCI EXPRESS	DESTINATION	USB3	DESTINATION
Lane 1	NGFF-1 WLAN + BT	7	None
Lane 2	CARD READER	8	None
Lane 3	None	9	None
Lane 4	None	10	None
Lane 5	None		
Lane 6	None		
Lane 7	None		
Lane 8	None		
Lane 9	SSD	SATA	DESTINATION
Lane 10	SSD	0A	SSD
Lane 11	SSD	1A	N/A
Lane 12	SSD	N/A	N/A
Lane 13	SSD	N/A	N/A
Lane 14	SSD	0B	None
Lane 15	SSD	1B	HDD
Lane 16	Alpine Ridge	2	None
		3	None

CLKOUT_PCIE	DESTINATION	CLKOUT_PCIE	DESTINATION
0	None	10	None
1	None	11	None
2	None	12	None
3	NGFF-1 WLAN	13	None
4	CARD READER	14	None
5	Thunderbolt	15	None
6	NGFF-2 SSD		
7	GPU		
8	None		
9	None		

Symbol Note :

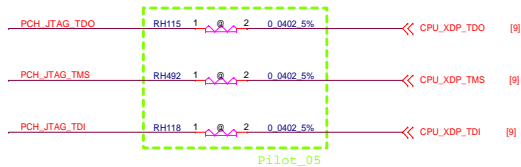
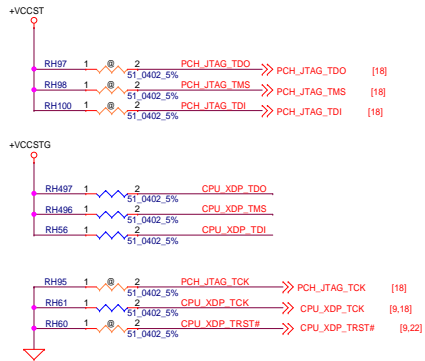


: means Digital Ground



: means Analog Ground





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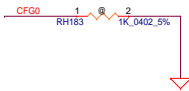




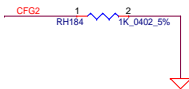


# CFG Straps for Processor

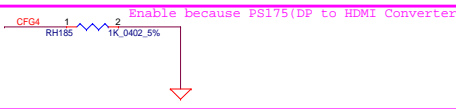
Stall reset sequence after CPU PLL lock until de-asserted	
CFG0	<p>★ 1 = (Default) Normal Operation; No stall.</p> <p>0 = Stall.</p>



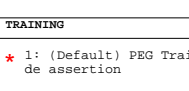
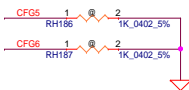
PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	<p>1: Normal Operation; Lane # definition matches socket pin map definition</p> <p>★ 0: Lane Reversed</p>



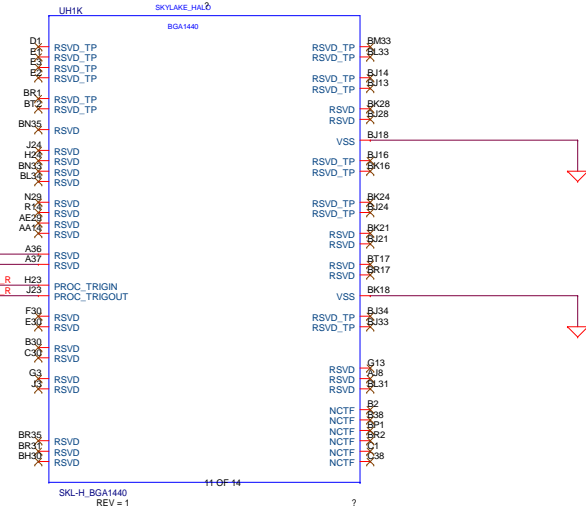
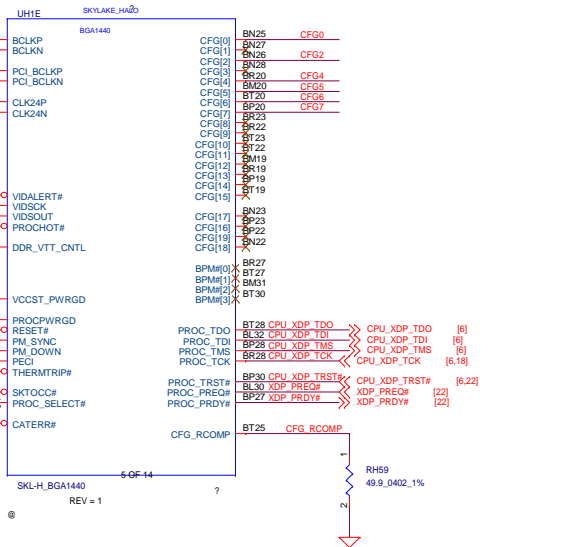
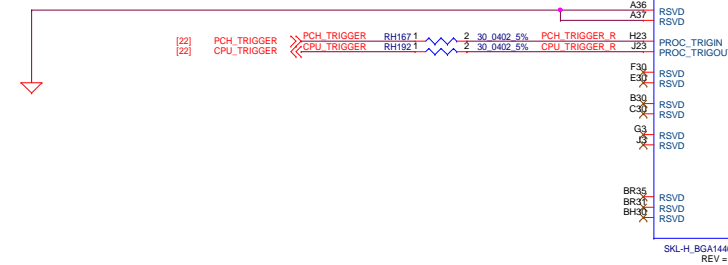
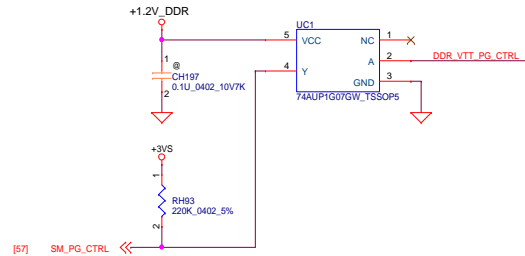
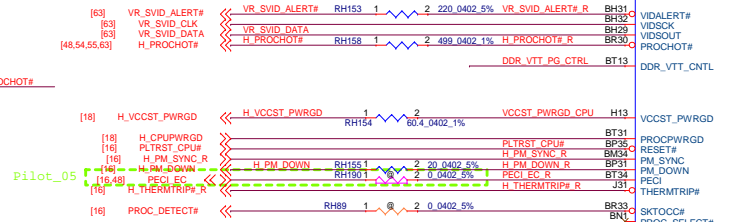
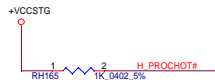
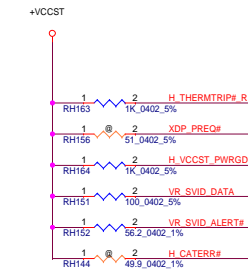
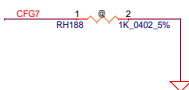
Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>★ 0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>

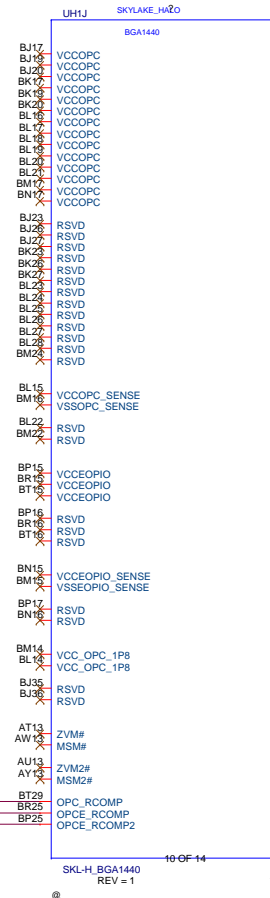
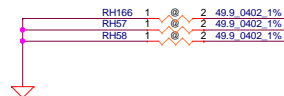
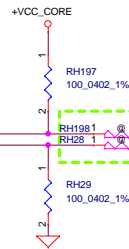
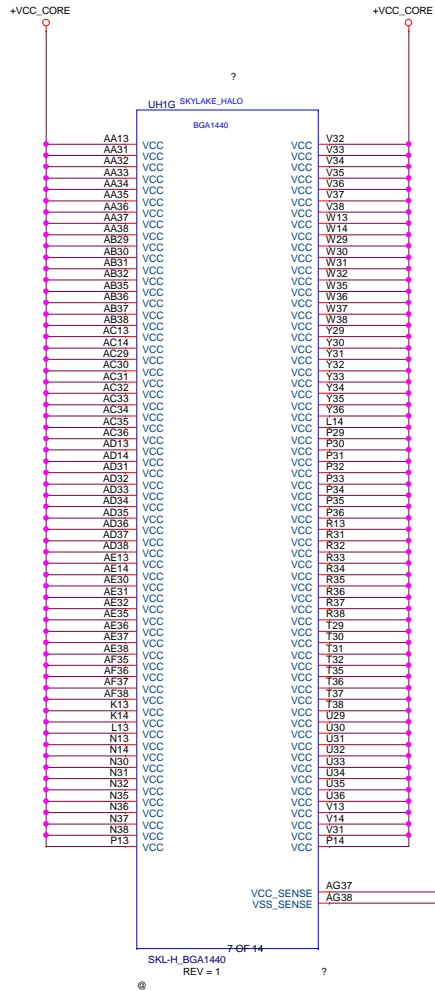


PCIe Port Bifurcation Straps	
CFG[6:5]	<p>★ 11: (Default) x16 - Device 1 functions 1 and 2 disabled</p> <p>10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled</p> <p>01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)</p> <p>00: x8,x4,x4 - Device 1 functions 1 and 2 enabled</p>

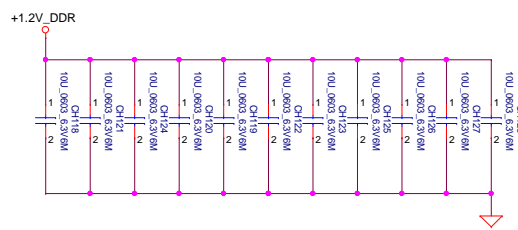
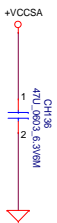
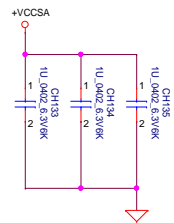
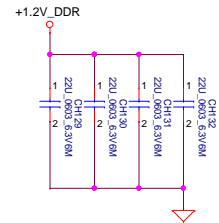
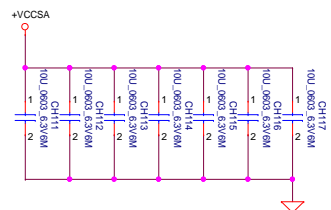
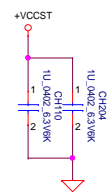
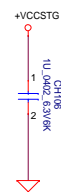
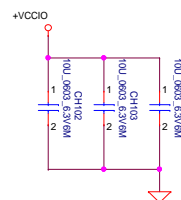
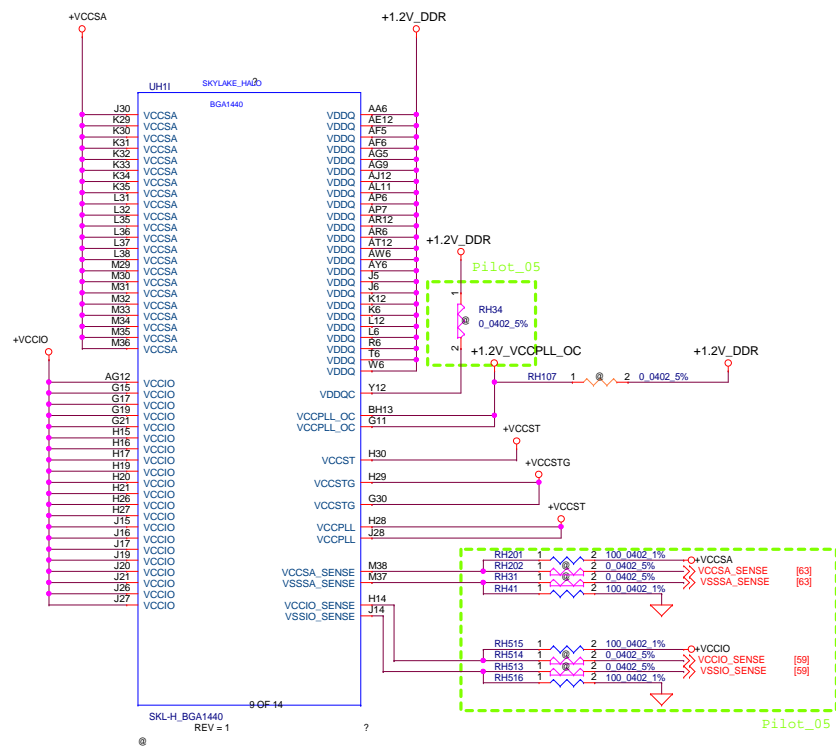


PEG DEFER TRAINING	
CFG7	<p>★ 1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>

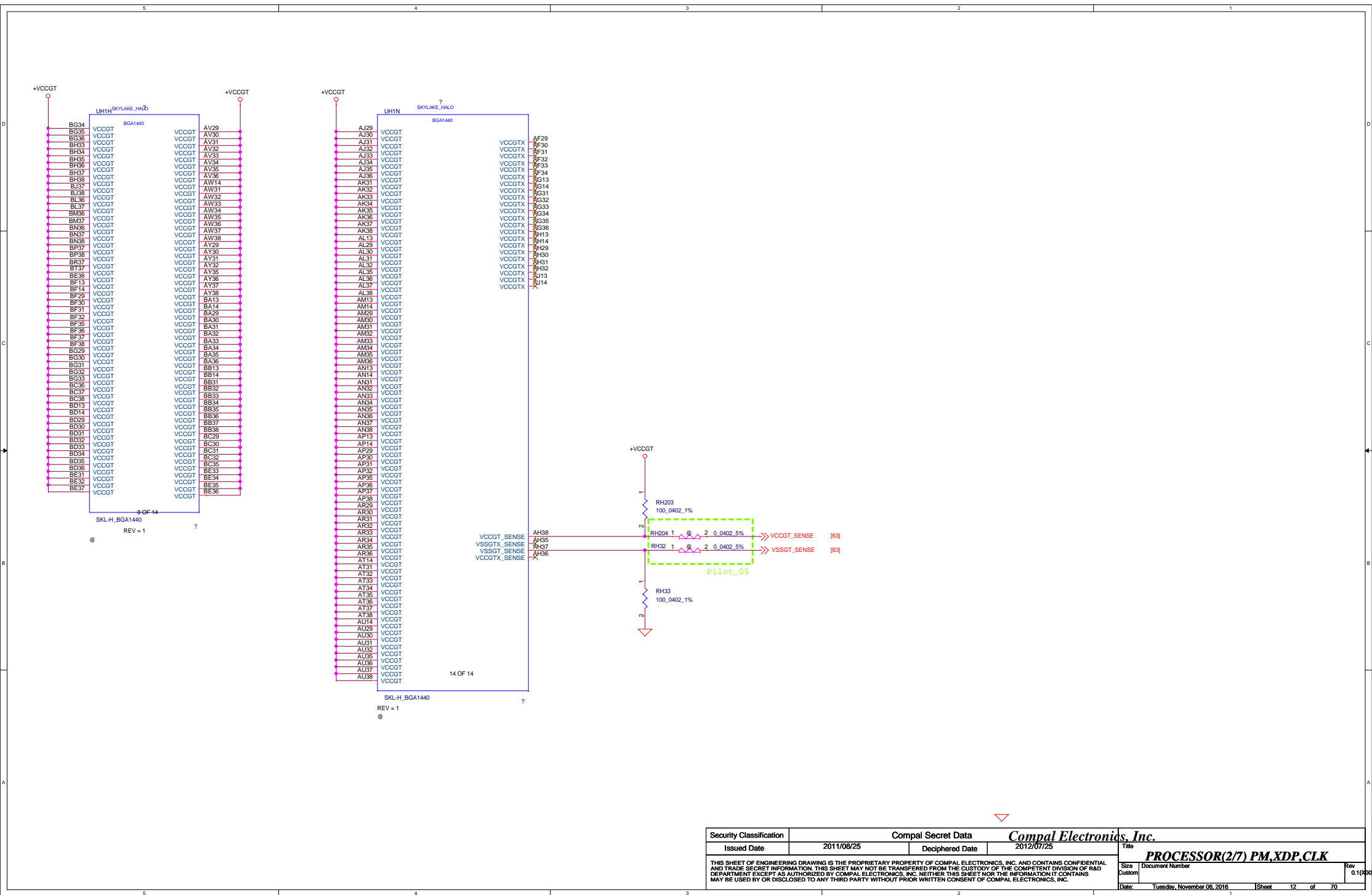




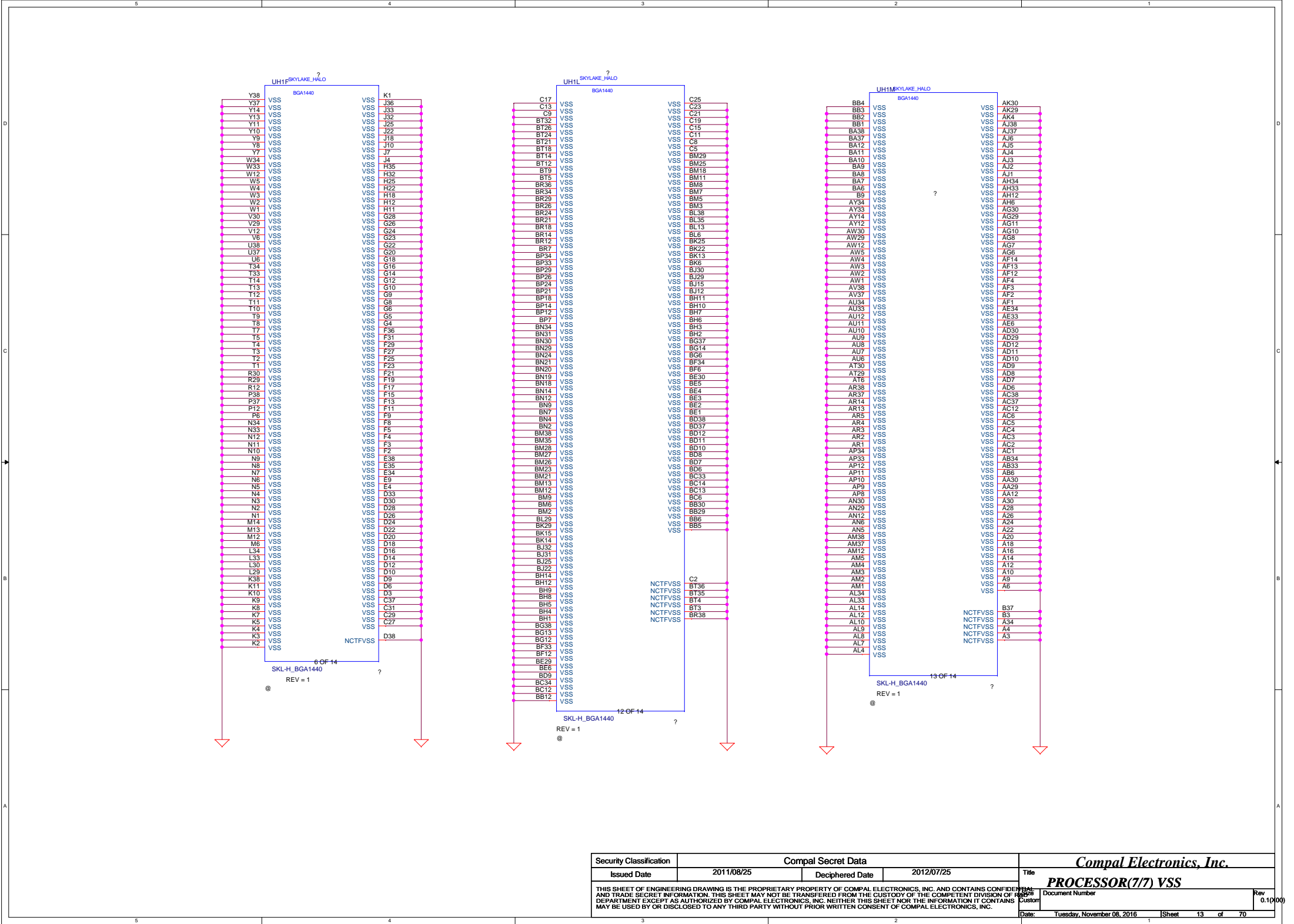
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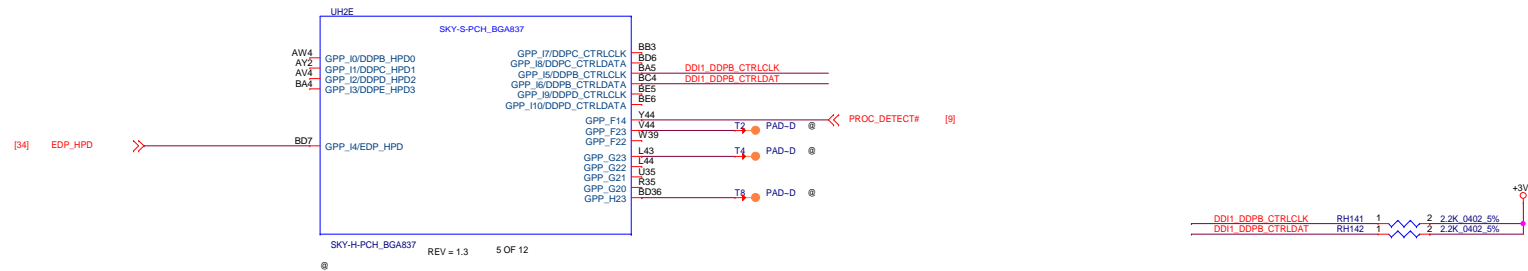
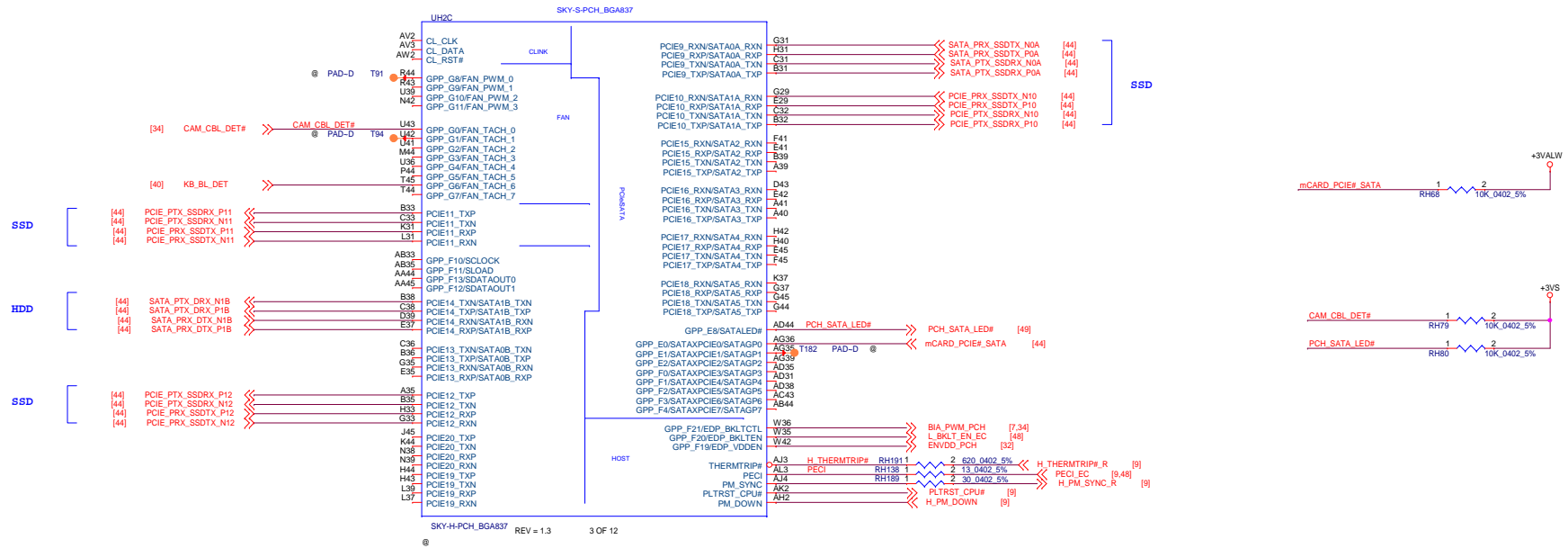


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**PCH Strap PIN**

**DisplayPort\* Disabling and Termination Guidelines**

Port	Strap	How to Enable Port?	How to Disable Port?
Port B	DDPB_CTRLCLK	Pull up to 3.3 V with 2.2-k $\Omega$ $\pm$ 5% resistor	No Connect
Port C	DDPC_CTRLCLK	Pull up to 3.3 V with 2.2-k $\Omega$ $\pm$ 5% resistor	No Connect
Port D	DDPD_CTRLCLK	Pull up to 3.3 V with 2.2-k $\Omega$ $\pm$ 5% resistor	No Connect







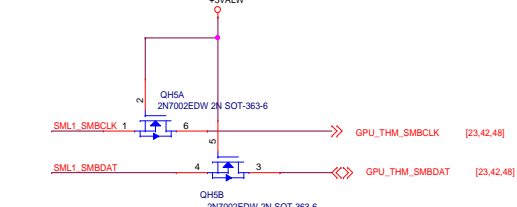
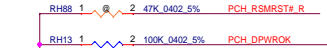
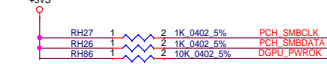
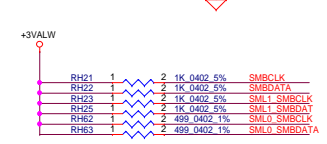
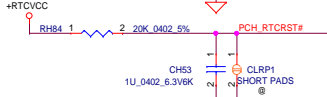
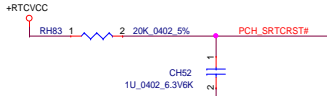
[37] HDA\_SDOIN\_AUDIO



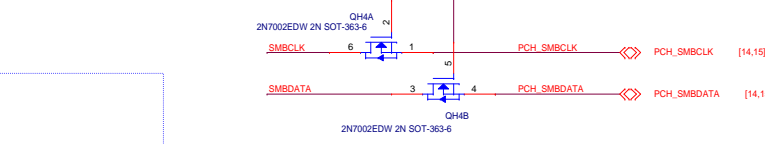
Close to PCH



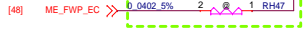
[7] AUD\_AZA\_CPU\_SDO\_R  
[7] AUD\_AZA\_CPU\_SDI\_R  
[7] AUD\_AZA\_CPU\_SCLK\_R



PCH to DDR



Service Mode Switch:  
Add a switch to ME\_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using PPT.

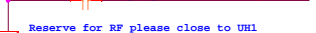
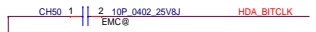
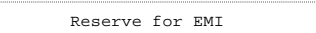
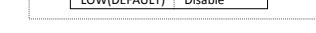
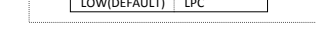
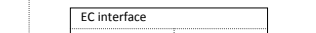
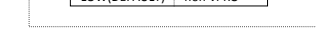
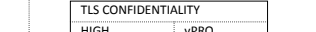
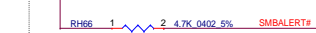
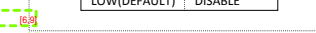
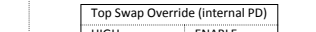
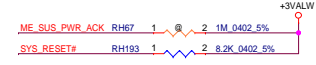
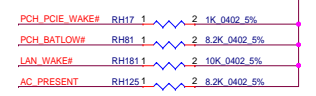
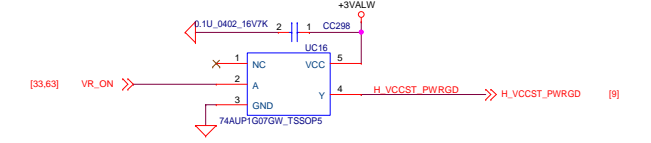


ME\_FWP PCH has internal 20K PD.

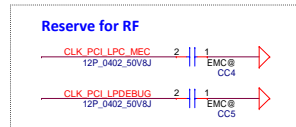
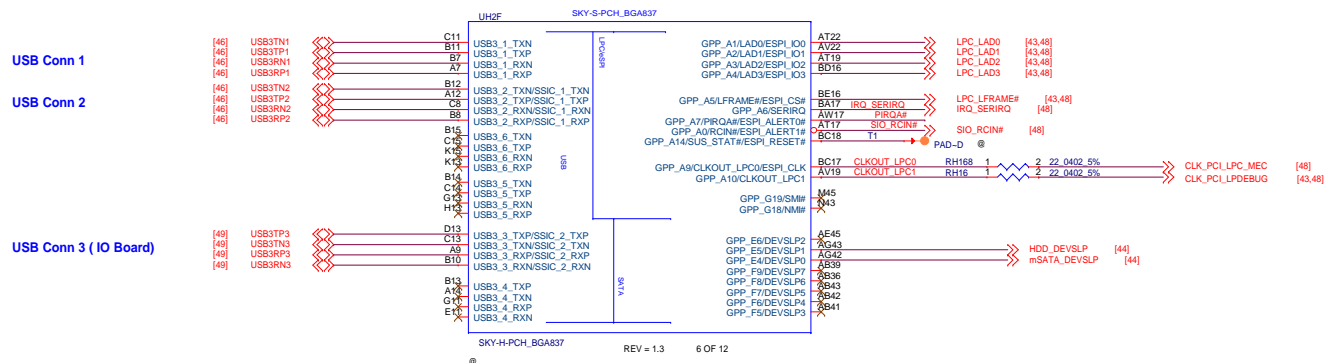
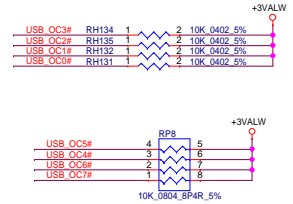
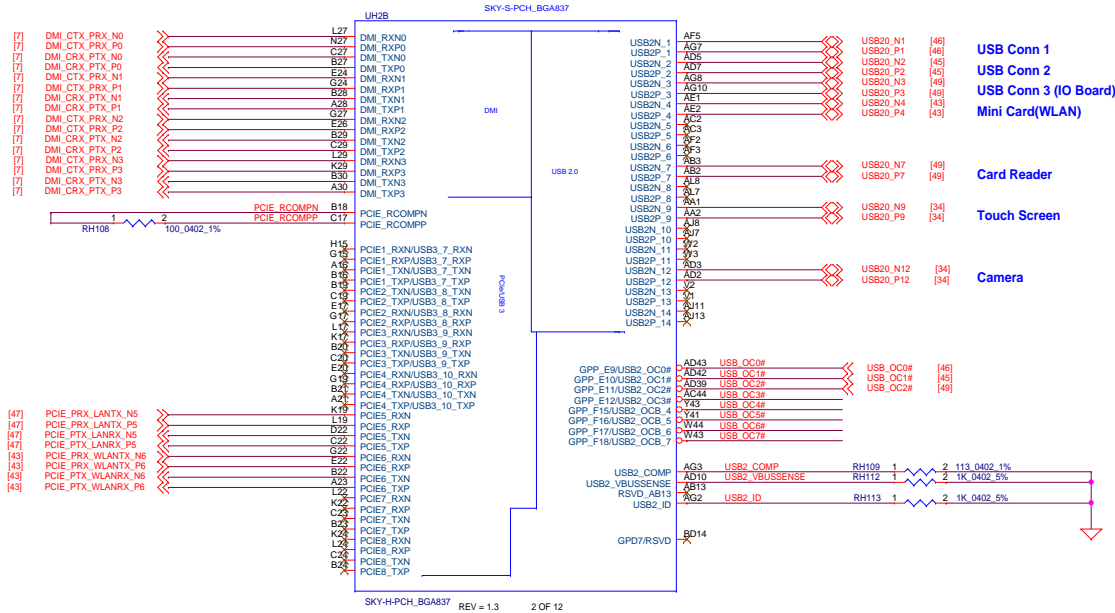
FLASH DESCRIPTOR SECURITY OVERRIDE

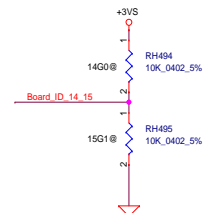
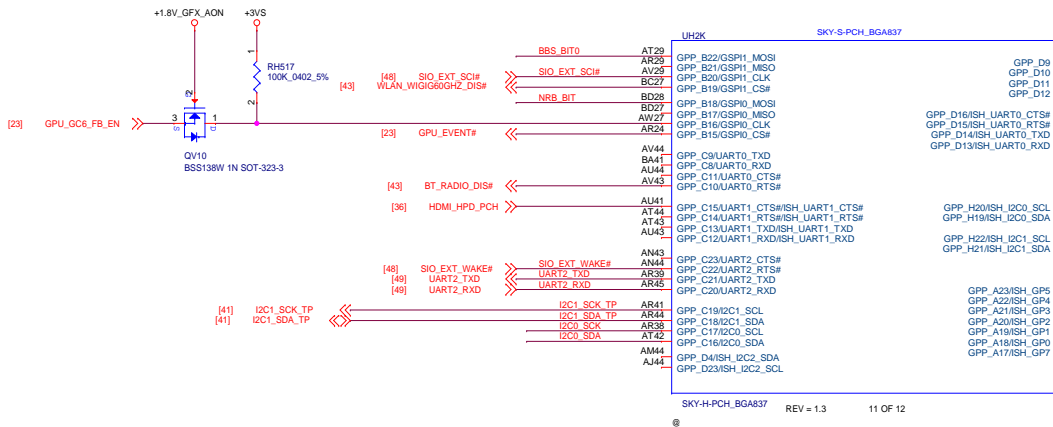
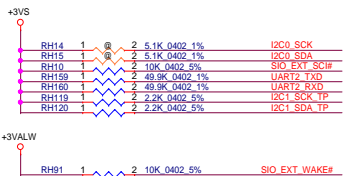
Disable ME Protect (ME can be updated) ----> Pin1 & Pin2 short  
Enable ME Protect (ME cannot be updated) --> Pin3 & Pin2 short(Default position)

Buffer with Open Drain Output For VTT power control

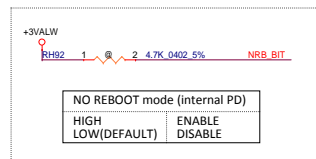
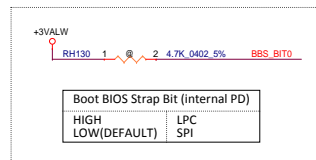
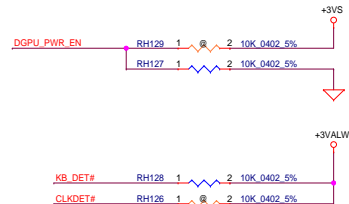


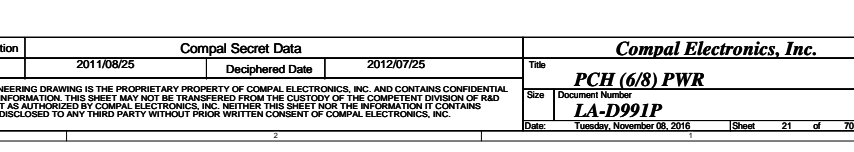
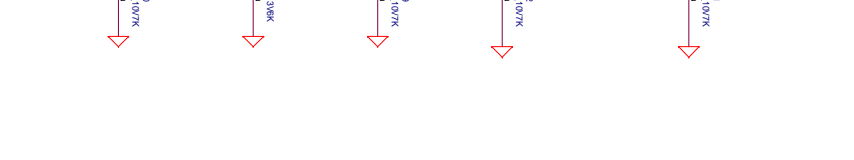
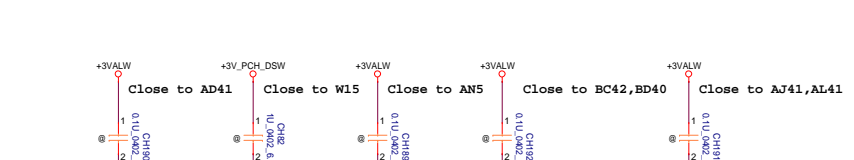
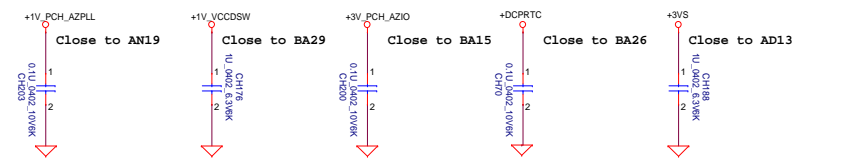
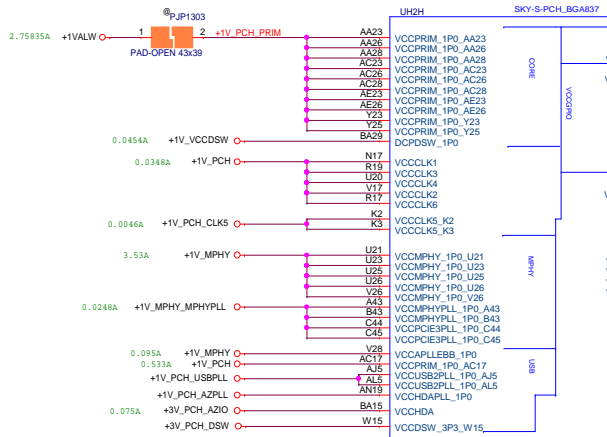
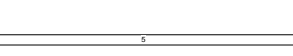
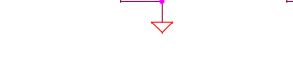
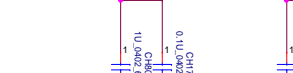
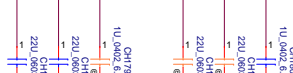
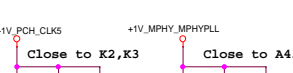
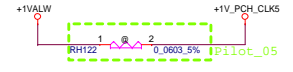
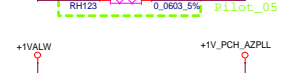
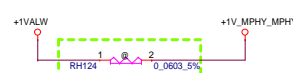
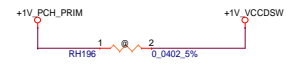
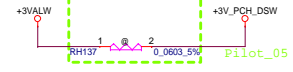
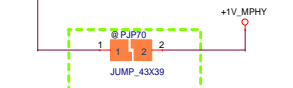
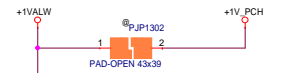
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Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	PCH (3/8) DMI, FDI, PM, GFX, DP
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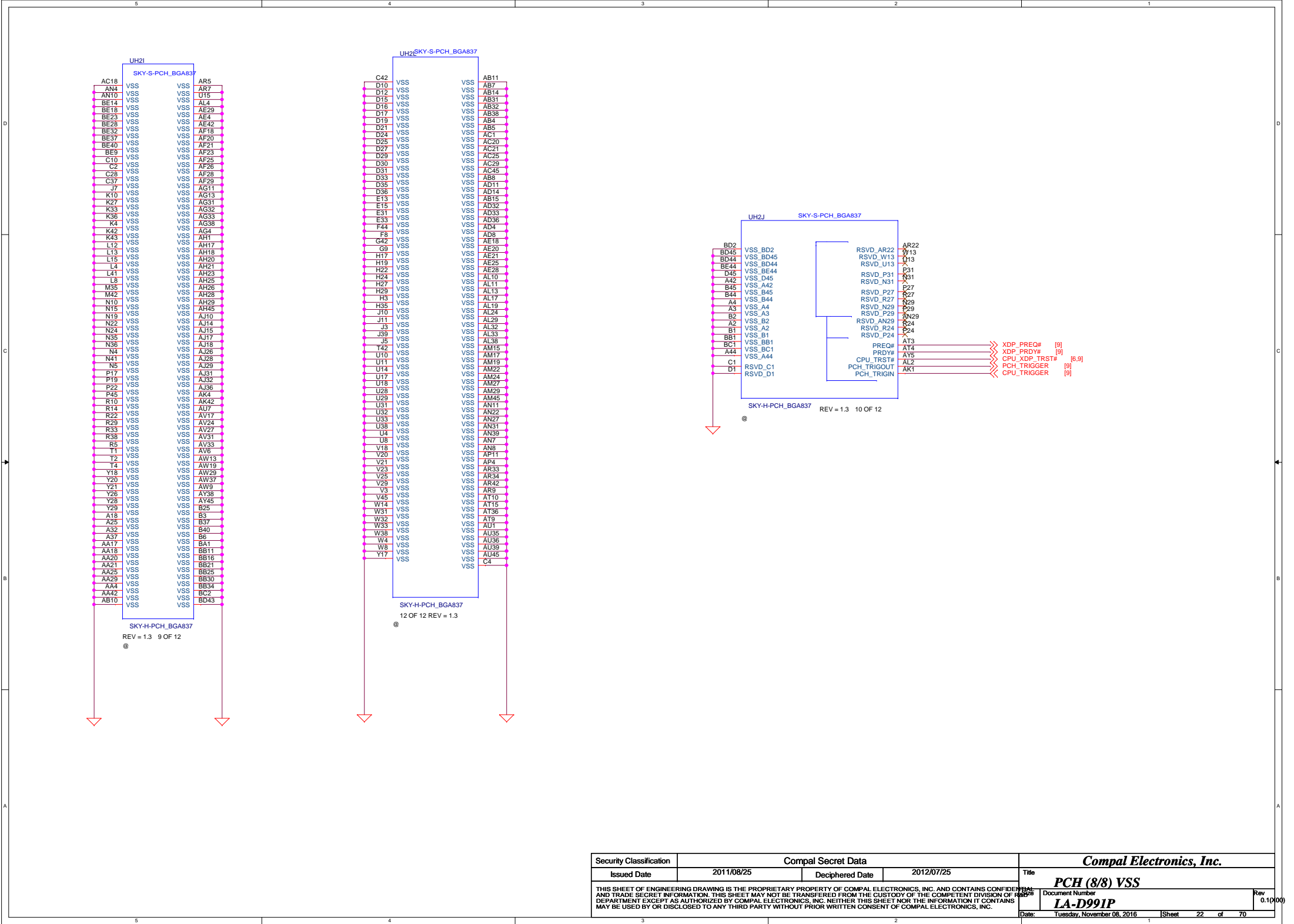


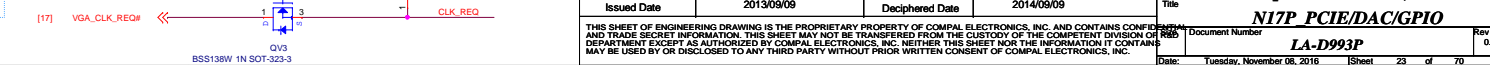
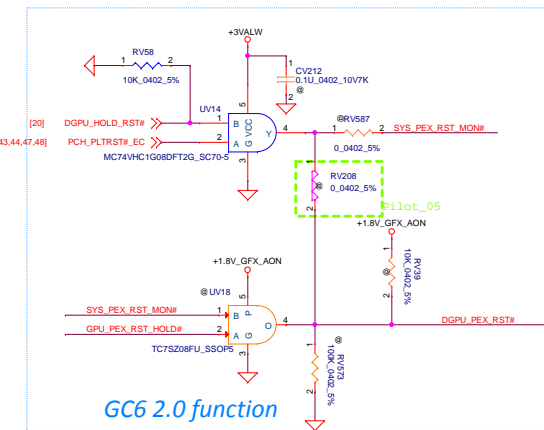
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LOW	15" & N16P_GX

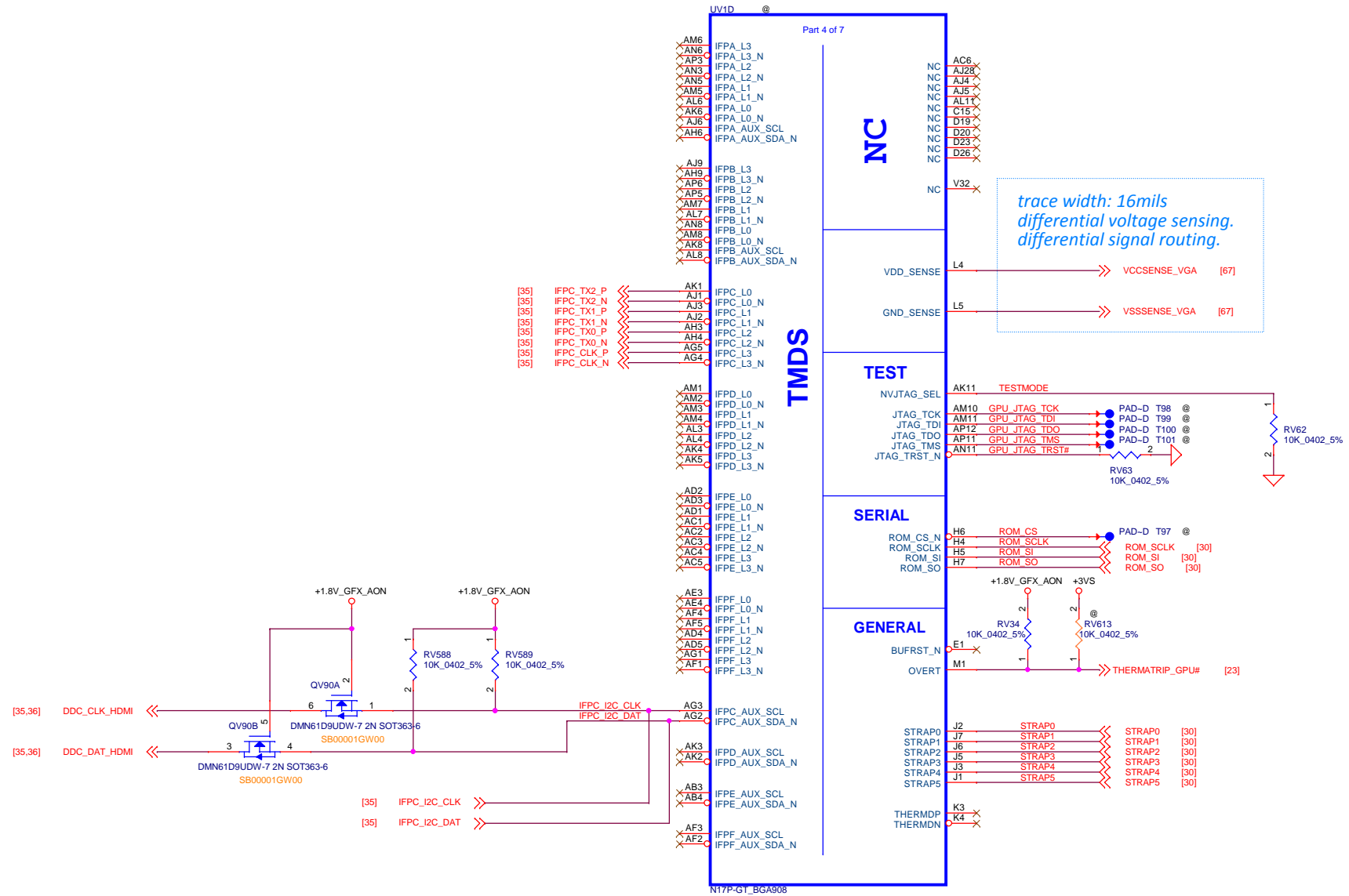




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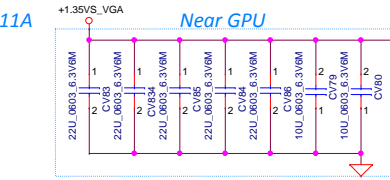


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										Rev	
										0.1(000)	
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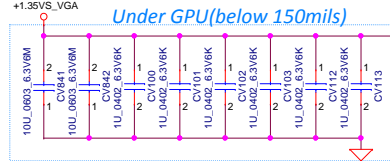
11A

Near GPU



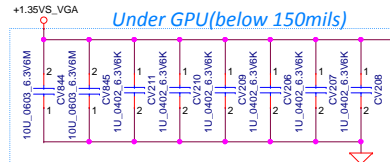
+1.35VS\_VGA

Under GPU(below 150mils)



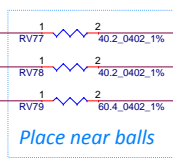
+1.35VS\_VGA

Under GPU(below 150mils)

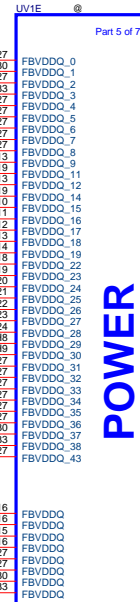


CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2 ohm
FB_CAL_x_PU_GND	40.2 ohm
FB_CAL_xTERM_GND	60.4 ohm

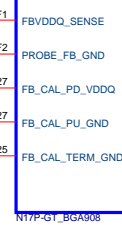
+1.35VS\_VGA



Place near balls



POWER

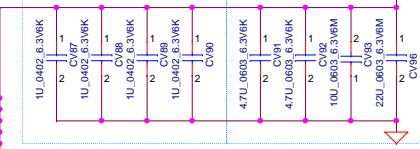


Under GPU

Near GPU

+1VS\_GFX

3A

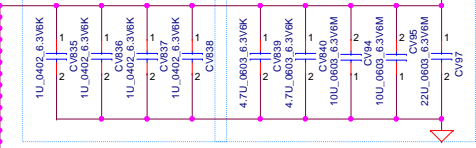


Under GPU

Near GPU

+1.8V\_GFX\_RUN

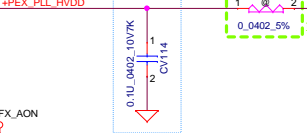
1A



Near GPU

+1.8V\_GFX\_RUN

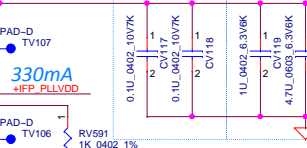
Pilot\_05



Under GPU

Near GPU

+1.8V\_GFX\_RUN

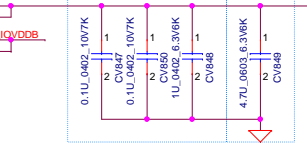


Under GPU

Near GPU

+1VS\_GFX

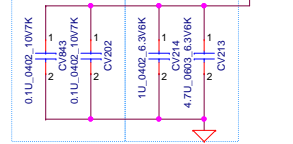
305mA



Under GPU

Near GPU

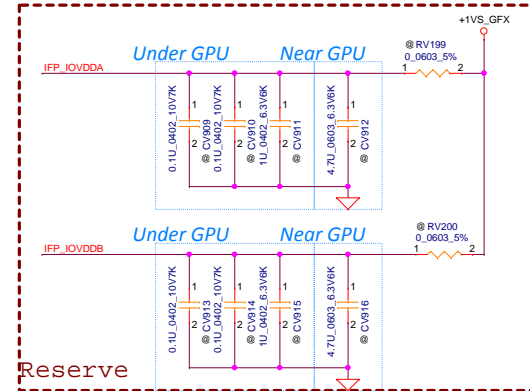
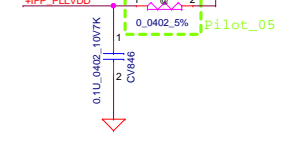
+1.8V\_GFX\_AON



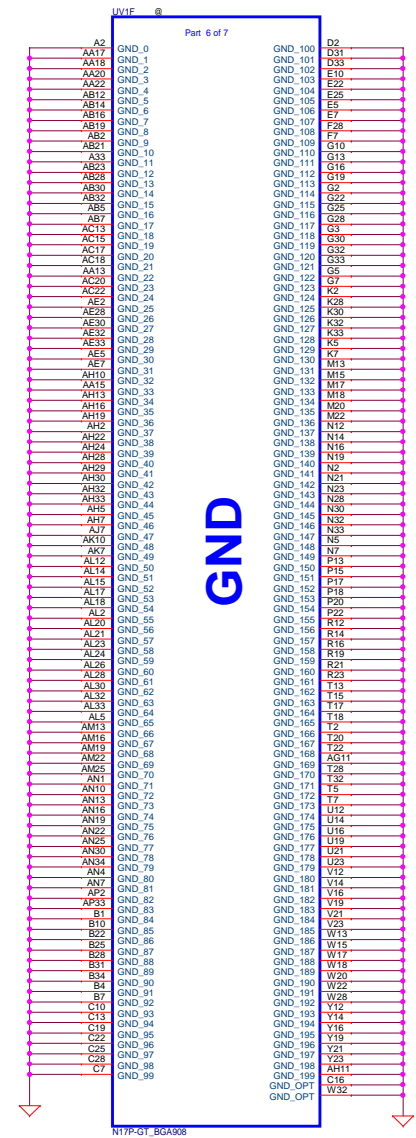
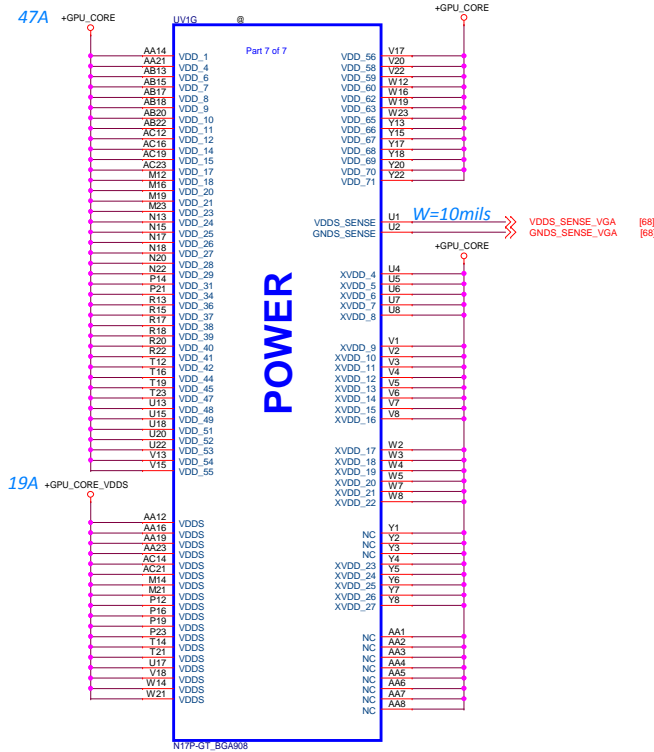
Under

+1.8V\_PLLVDD

Pilot\_05



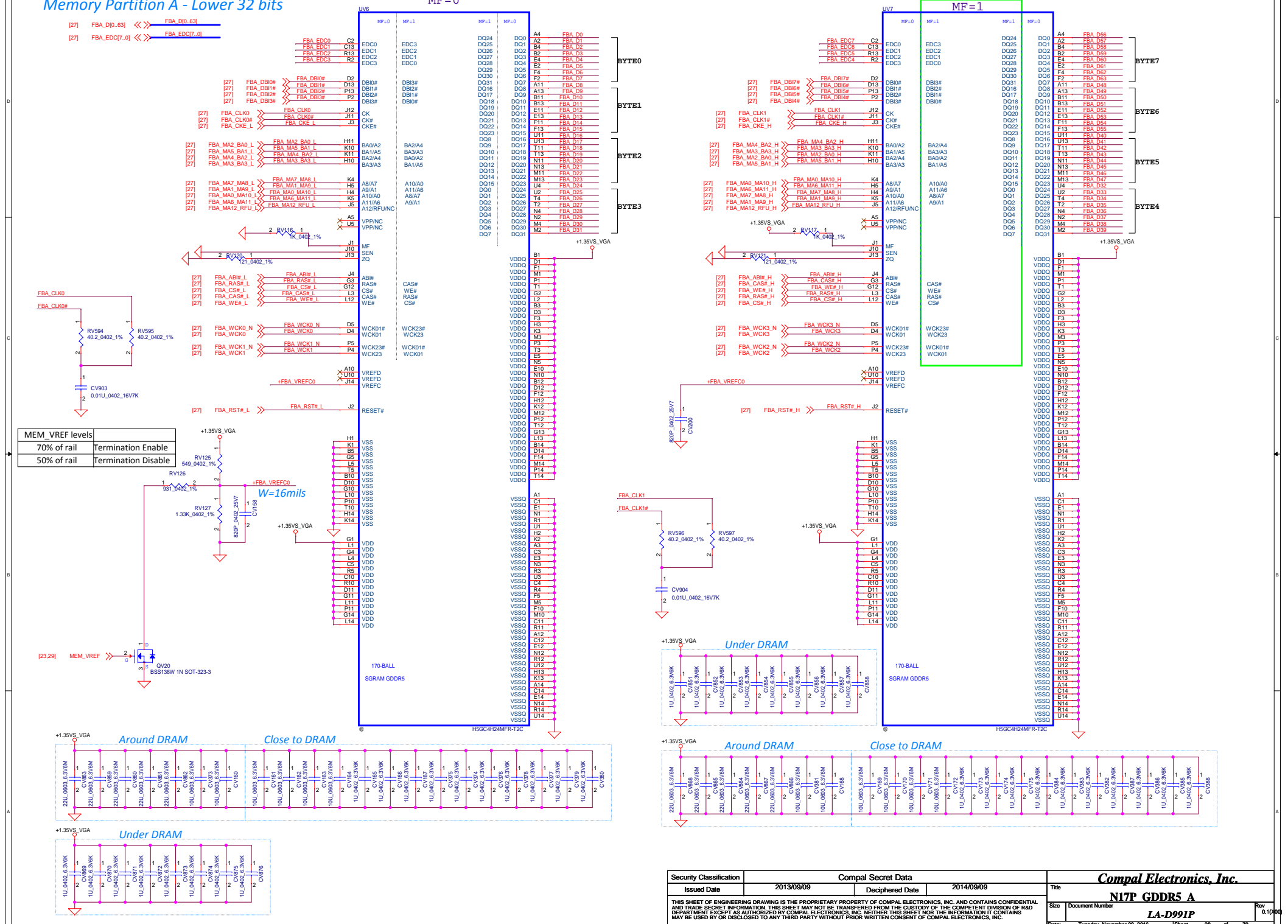
Reserve



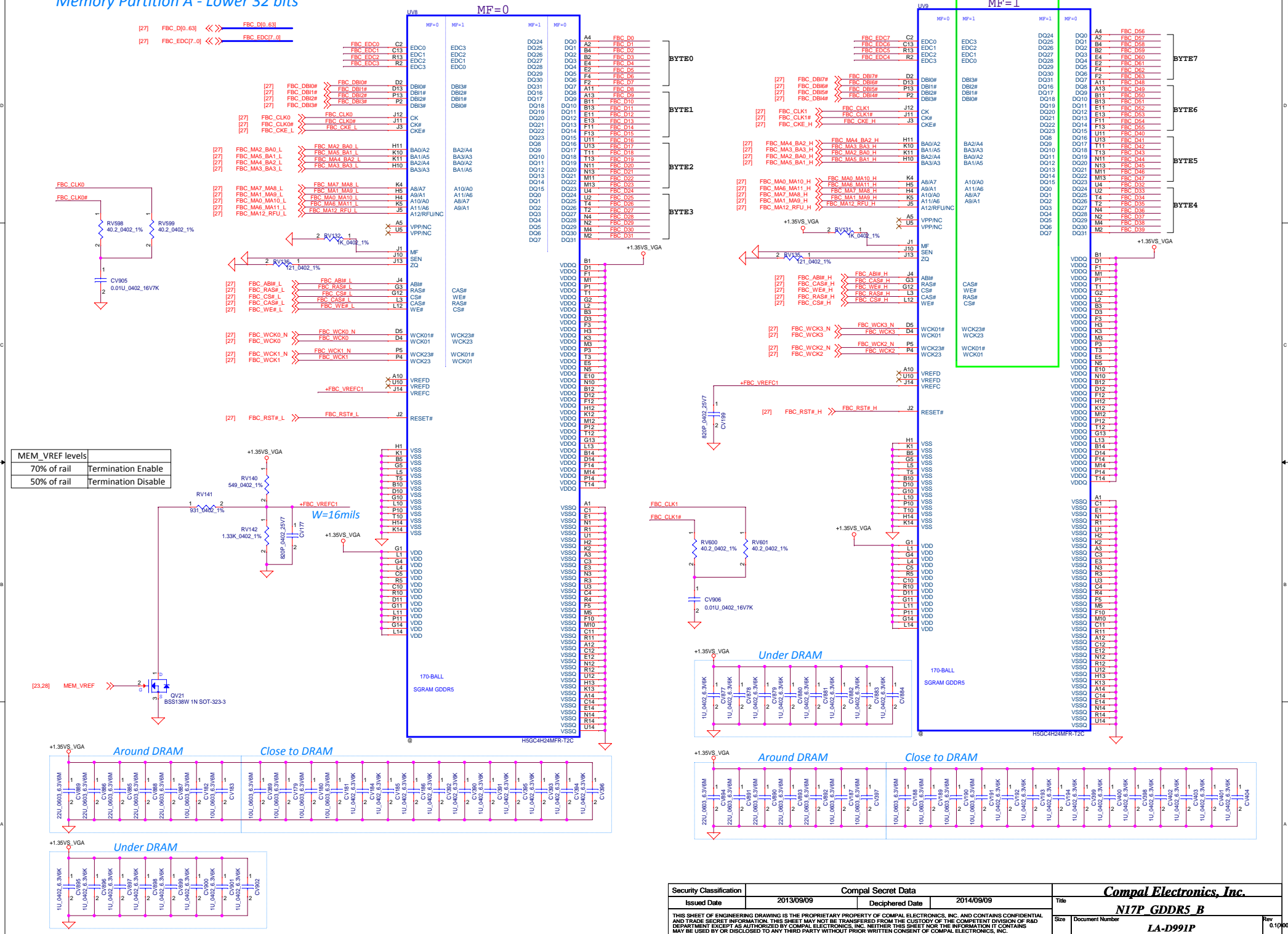
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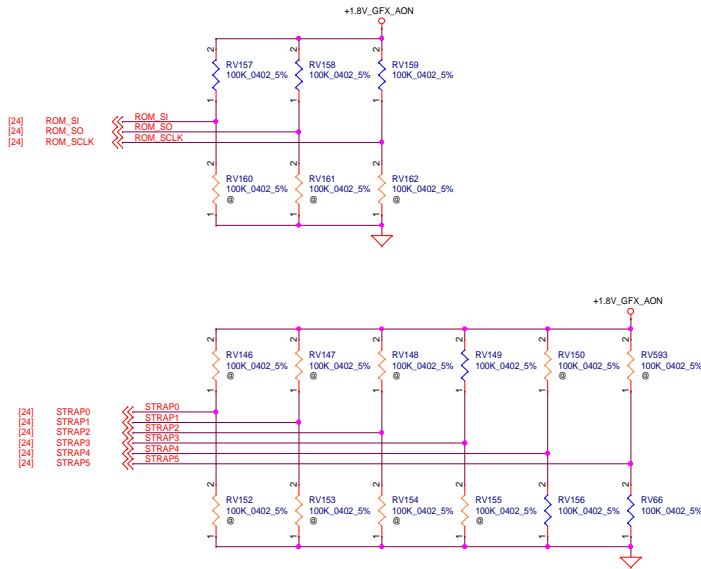
Memory Partition A - Lower 32 bits



# Memory Partition A - Lower 32 bits







SMB_ALT_ADDR	
Low	Single GPU
High	Dual GPU
DEVID_SEL	
Low	Original Device ID
High	Re-brand Device ID
VGA_DEVICE	
Low	3D Device
High	VGA Device
PCIE_CFG	
Low	Normal signal swing
High	Reduce the signal amplitude

Table 5.2 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 1. N17P-G0/-G1 GDDR5 Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Allowed Memory Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
GDDR5	1.35V/ 1.35V and 1.5V/ 1.5V See Note 2	8 Gb	256Mx32	Samsung	K4G80325FB-HC28	B-die	0x0	3500	N/A	Production candidate
				Micron	MT51J256M32HF-70-A	A-die	0x1	3500	N/A	Production candidate
				Hynix	H5GQ8H24MJR-R0C	M-die	0x2	3500	N/A	Post-production candidate

**Note:**

- For N17P-Gx, the maximum allowable memory case temperature is 85 °C.
- N17P-Gx runs WCLK up to 3000 MHz with FBVDD=1.35V. DVS is required to run WCLK > 3000 MHz.

Table 5.5 SMB ALT\_ADDR, DEVID\_SEL, PCIE\_CFG, VGA\_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

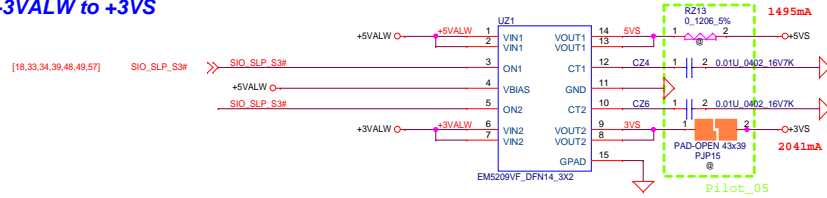
Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
8	H	H	H	ENABLED	disabled	disabled	disabled

Total Display Links (HDMI, DP or DVI)					See This Row of <a href="#">Table 5.5</a>
	Total Enabled for Audio (HDMI, DP or DVI)				
		Is eDP Supported on:			
		IFPA or IFPB?	IFPC or IFPD?	IFPE or IFPF?	
1	1	--	--	--	8

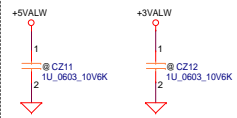
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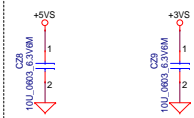
**+5VALW to +5VS**  
**+3VALW to +3VS**



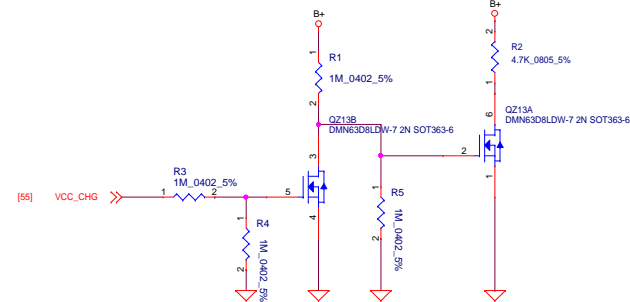
Close UZ1



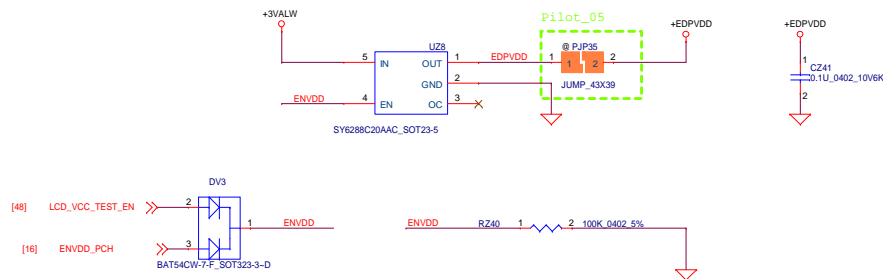
Close UZ1



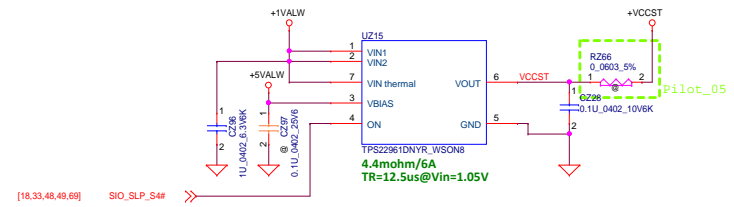
## B+ Discharge



## eDP & Camera Load Switch



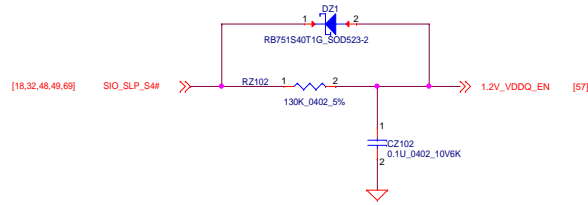
## +VCCST Load Switch



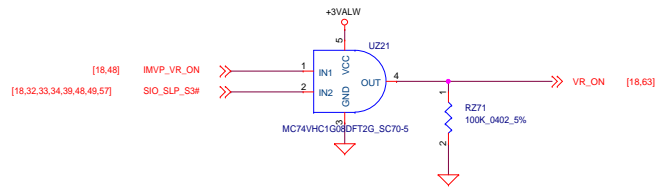
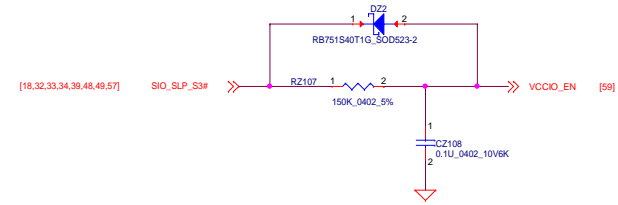
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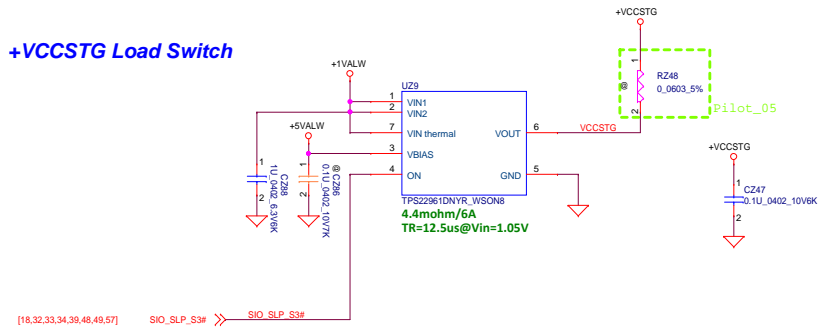
### +1.2V\_DDR Enable



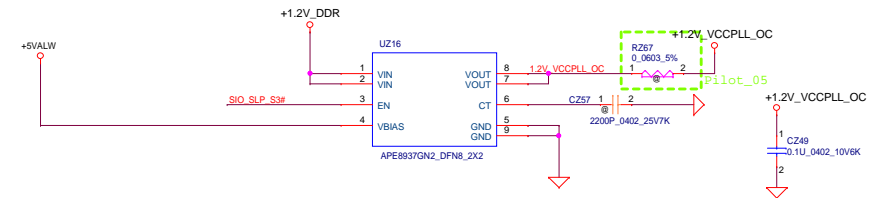
### +VCCIO Enable



### +VCCSTG Load Switch

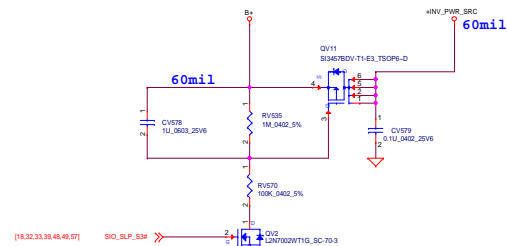


### +VCCPLL\_OC Load Switch

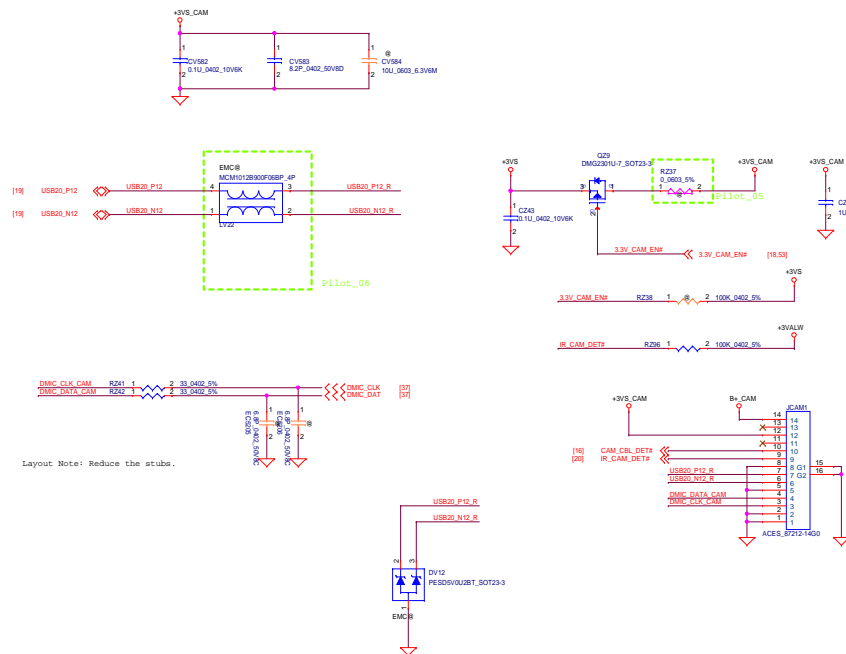


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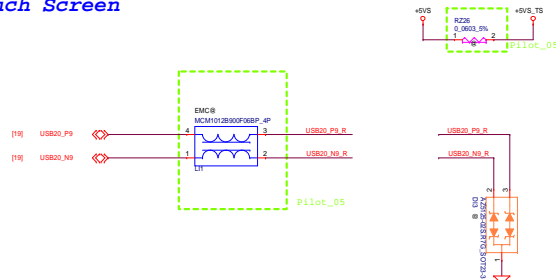
## LCD backlight PWR CTRL

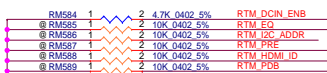
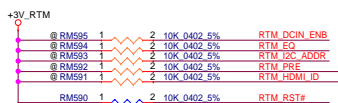
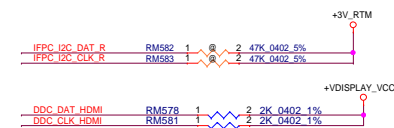
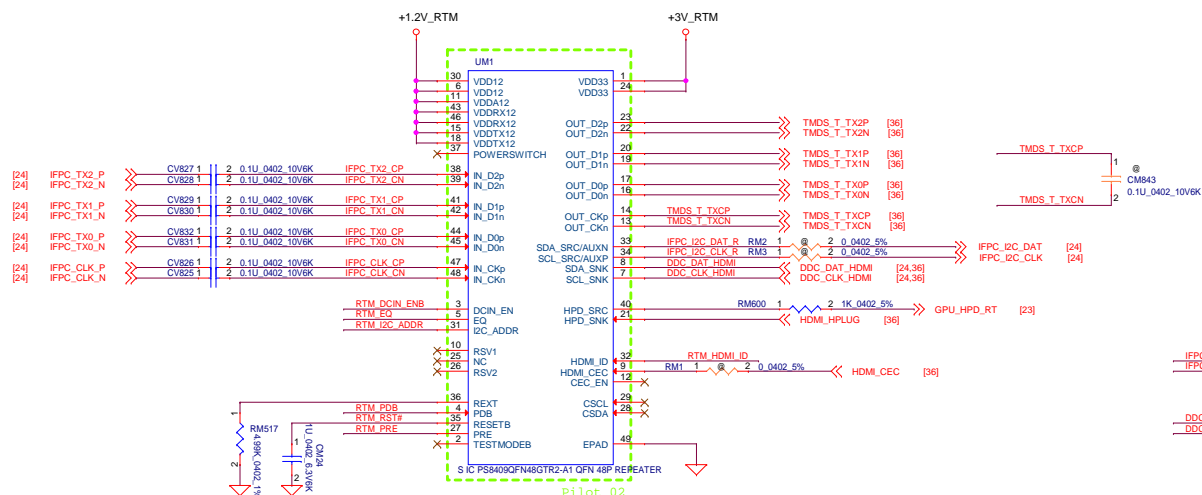
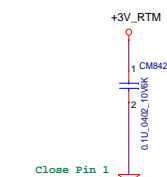
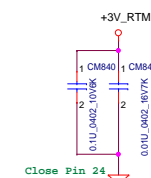


## CCD +DMIC Conn.



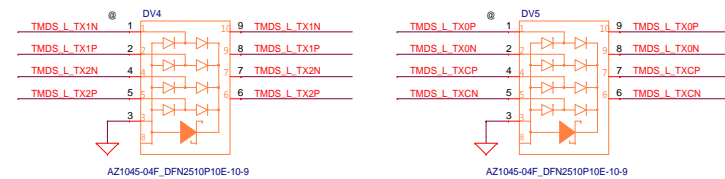
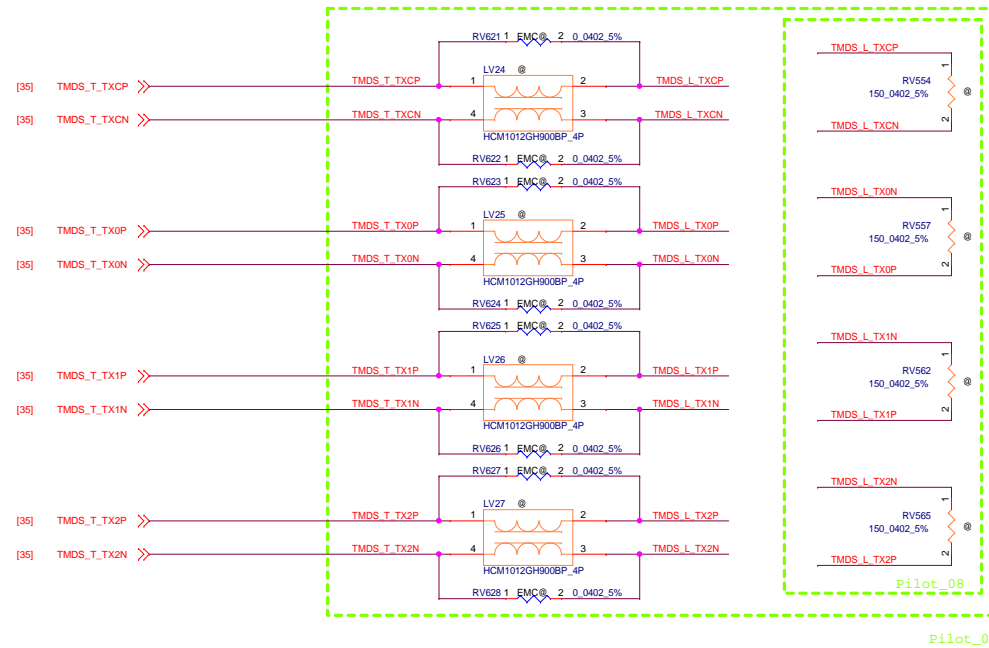
## Touch Screen



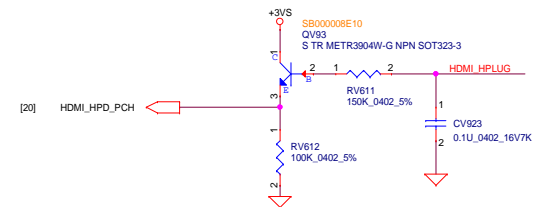
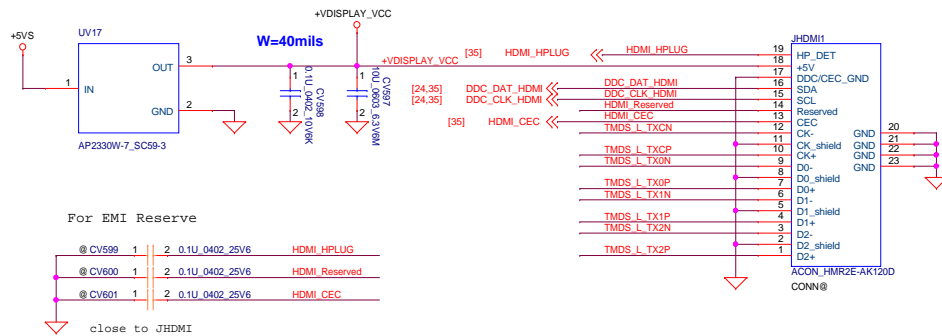


Place close to JHDMI1

Place between ESD and CM-Choke

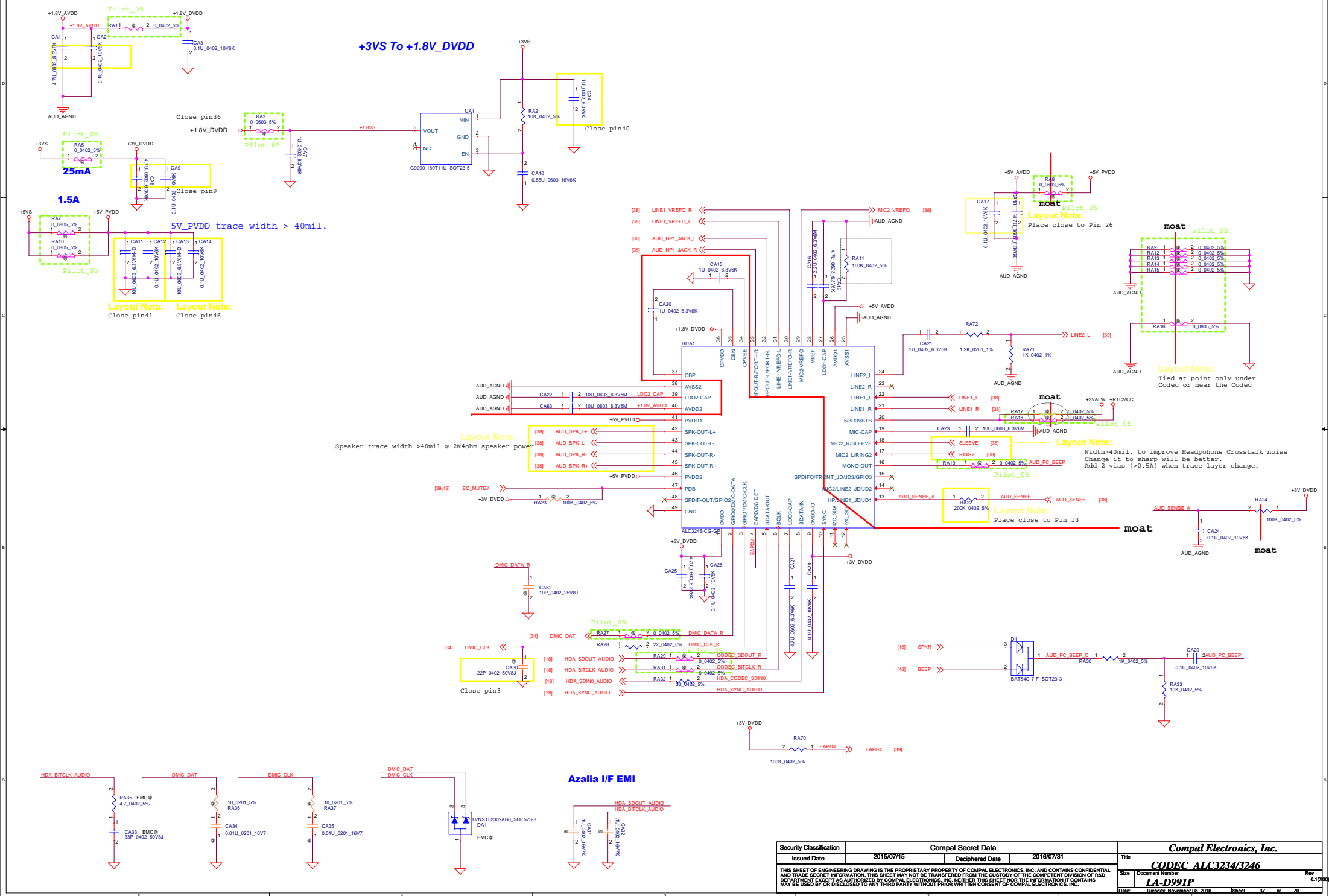


HDMI conn



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				HDMI	
				Size	Document Number
				Custom	LA-D991P
				Rev	0.1/000
Date:		Wednesday, November 09, 2016		Sheet	36 of 70

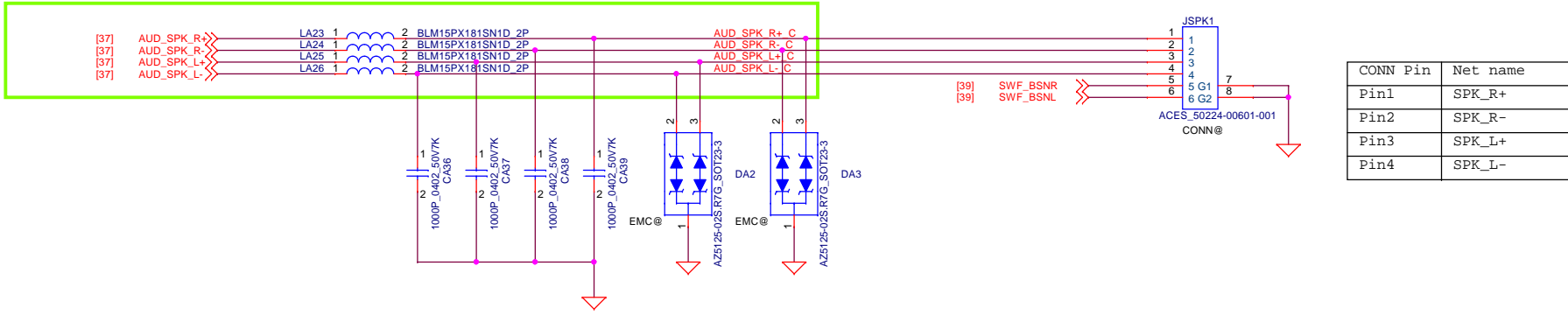
5  
Main Func = Audio



Main Func = Audio

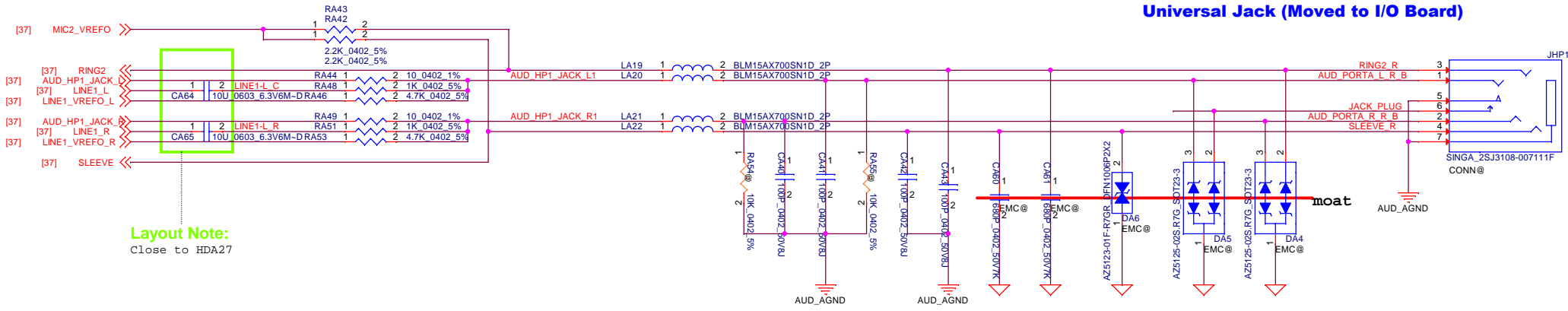
Layout Note:  
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

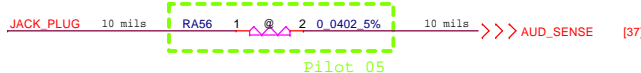


CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

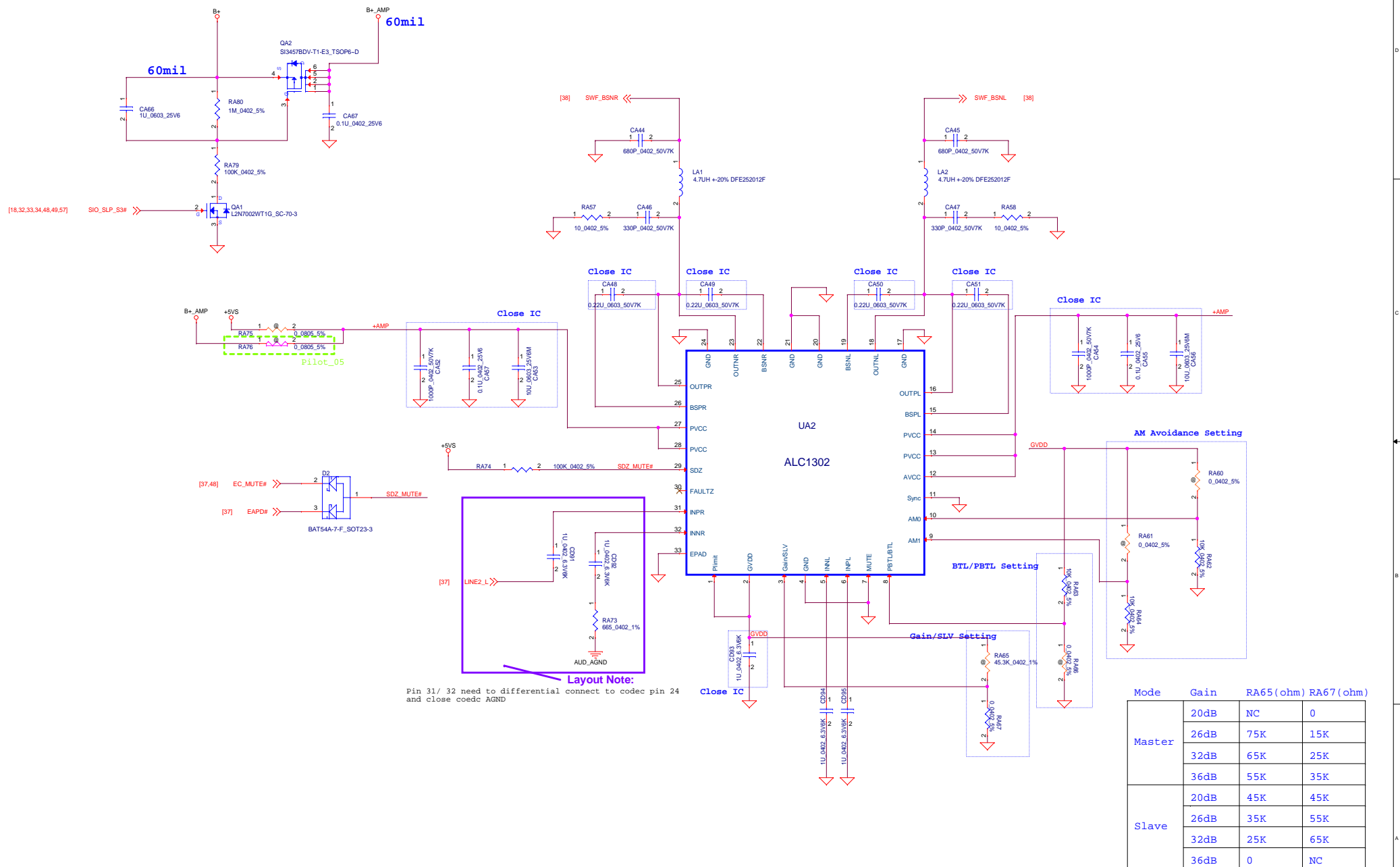
Universal Jack (Moved to I/O Board)



Layout Note:  
Close to HDA27

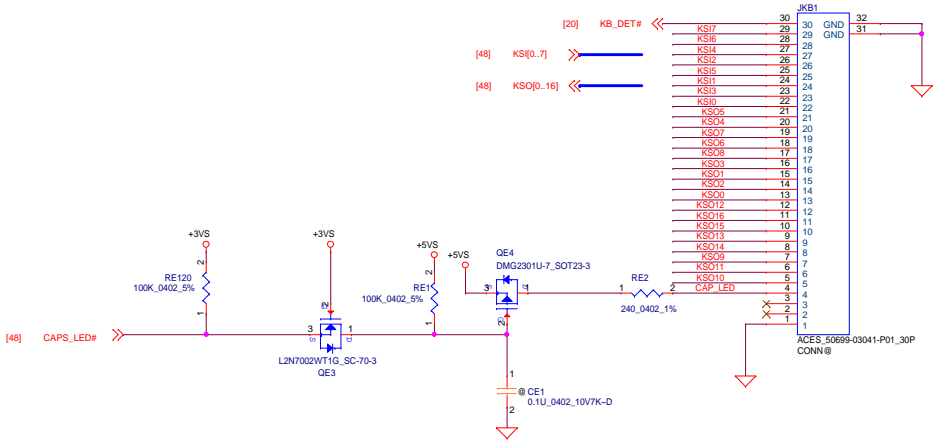


## Subwoofer AMP

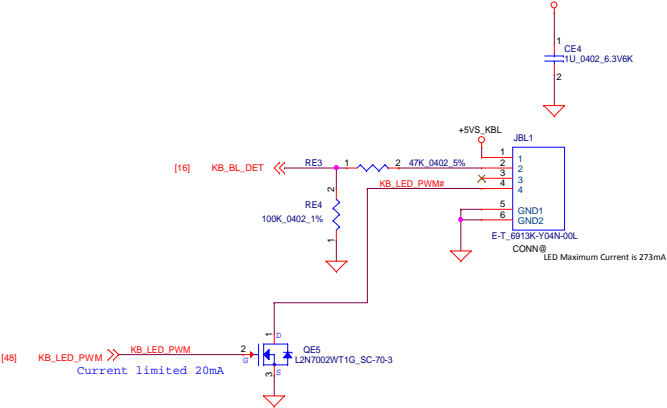


Mode	Gain	RA65 (ohm)	RA67 (ohm)
Master	20dB	NC	0
	26dB	75K	15K
	32dB	65K	25K
	36dB	55K	35K
Slave	20dB	45K	45K
	26dB	35K	55K
	32dB	25K	65K
	36dB	0	NC

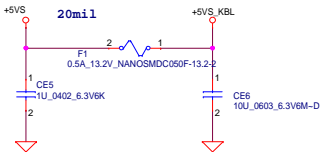
# Connector for Keyboard



# Connector for Keyboard Backlight

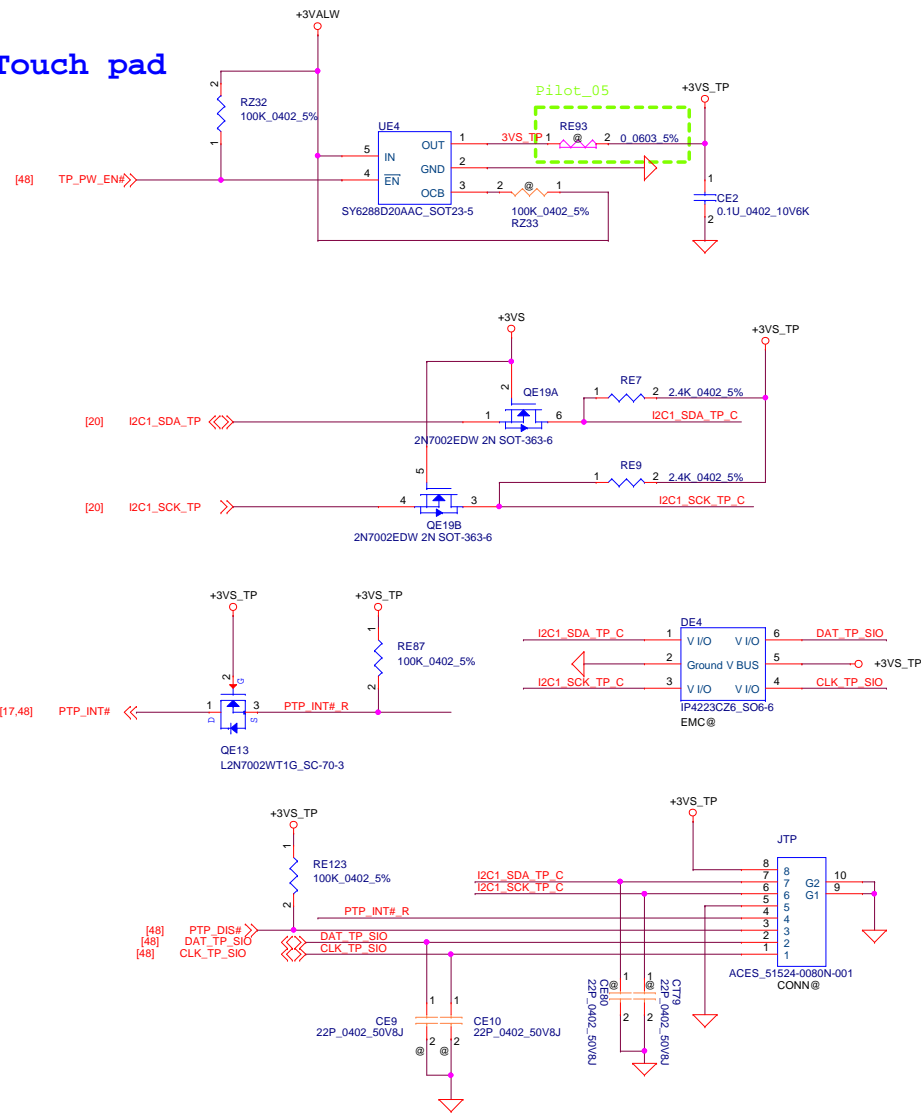


# Fuse for Backlight



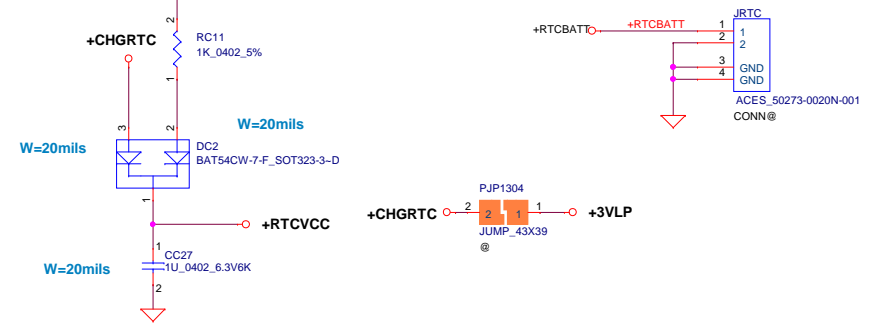


## Touch pad

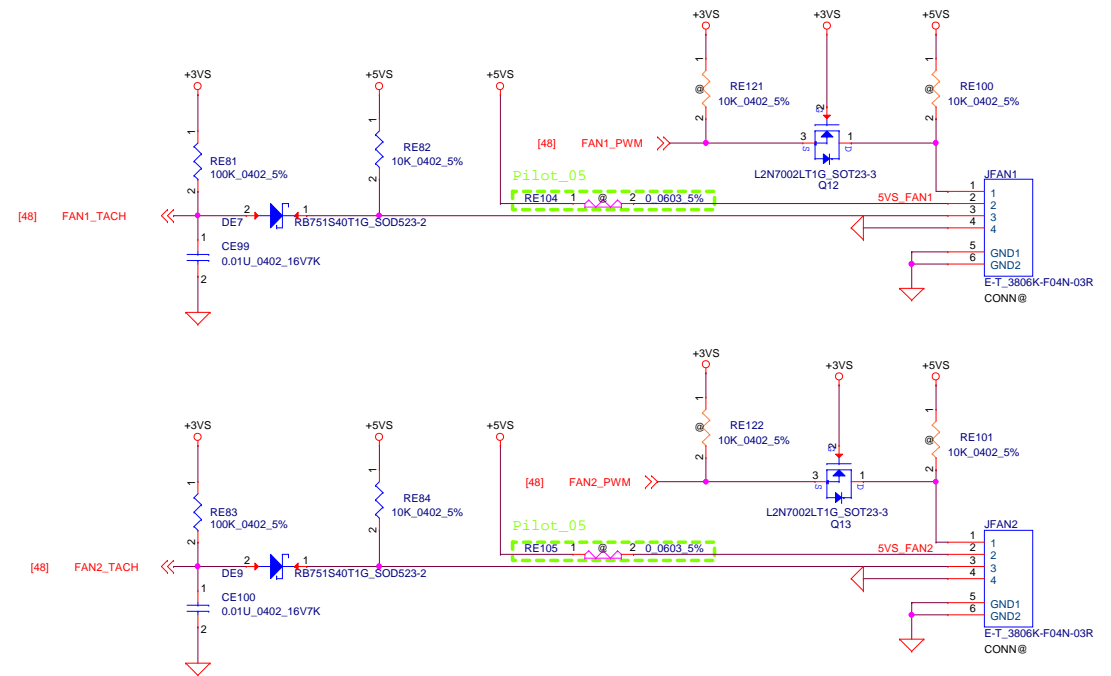


## RTC Battery non- Charge Function

### RTC Battery +RTCBATT



## PWM FAN

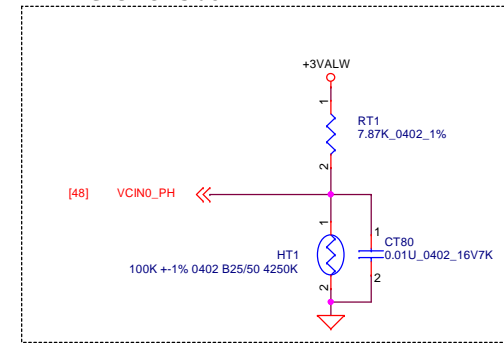
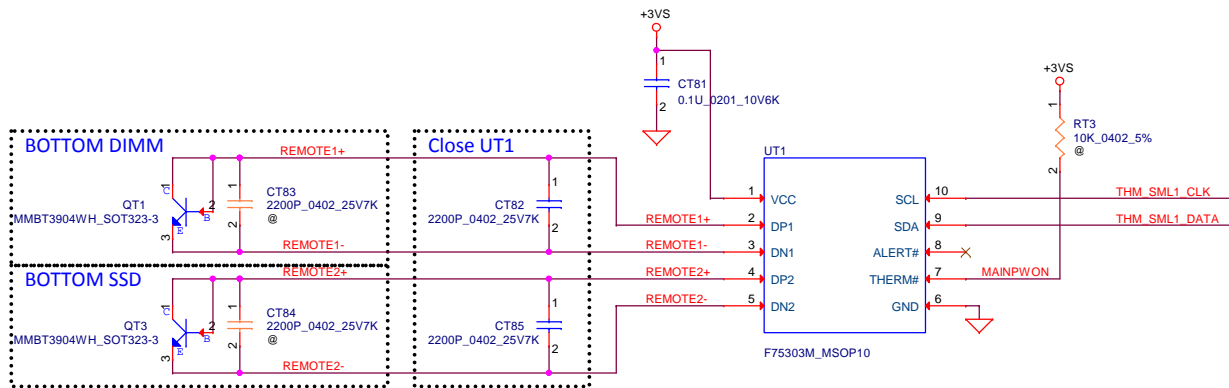


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						Document Number				Rev	
						LA-D991P				0.1(X00)	
						Date:		Tuesday, November 08, 2016		Sheet 41 of 70	

Compal Electronics, Inc.

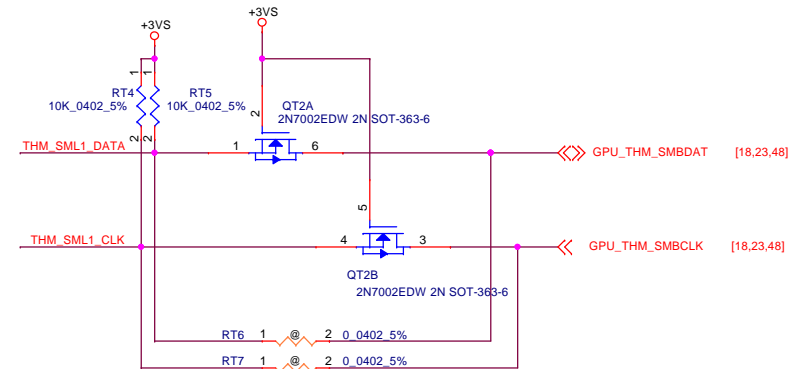
FAN/TP/KB/PWR SW

Fintek thermal sensor  
placed TOP near between GPU & CPU

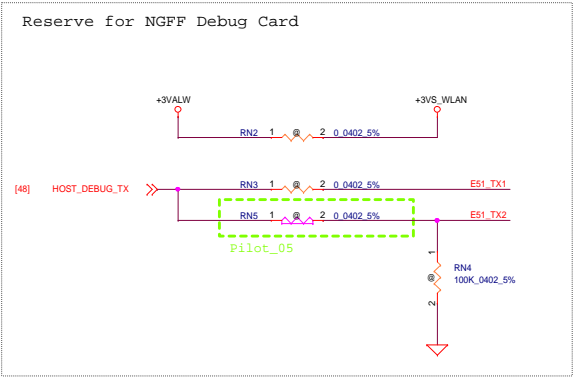
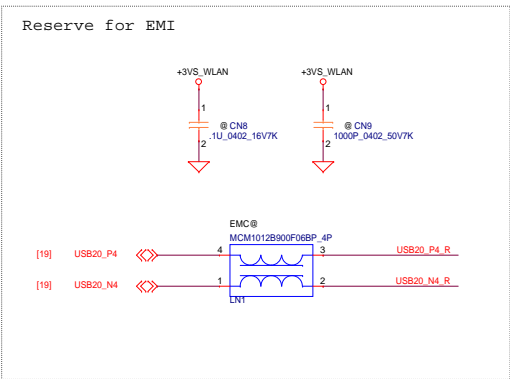
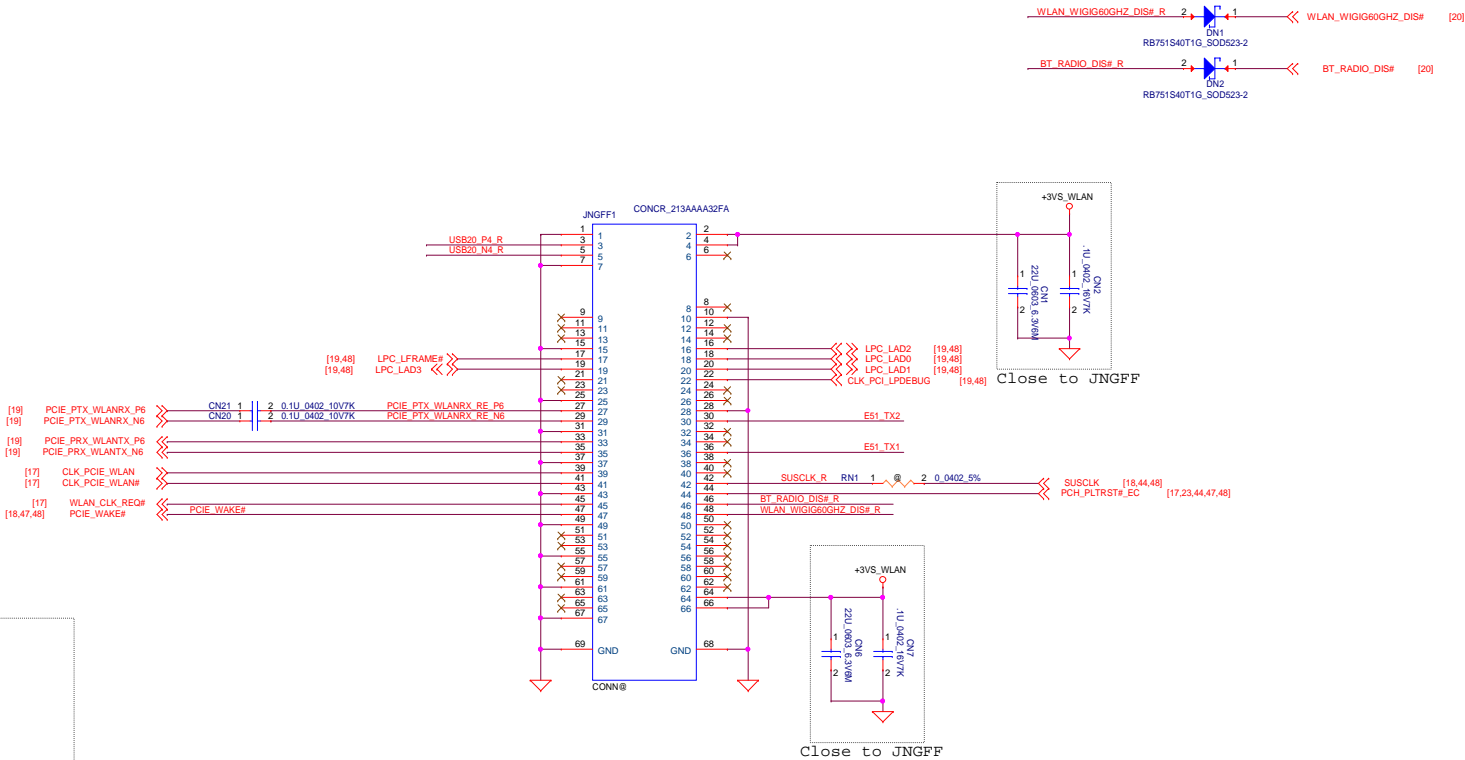
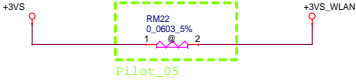


REMOTE1,2 (+/-) :  
Trace width/space:10/10 mil  
Trace length:<8"

Address 1001\_101xb  
2nd source  
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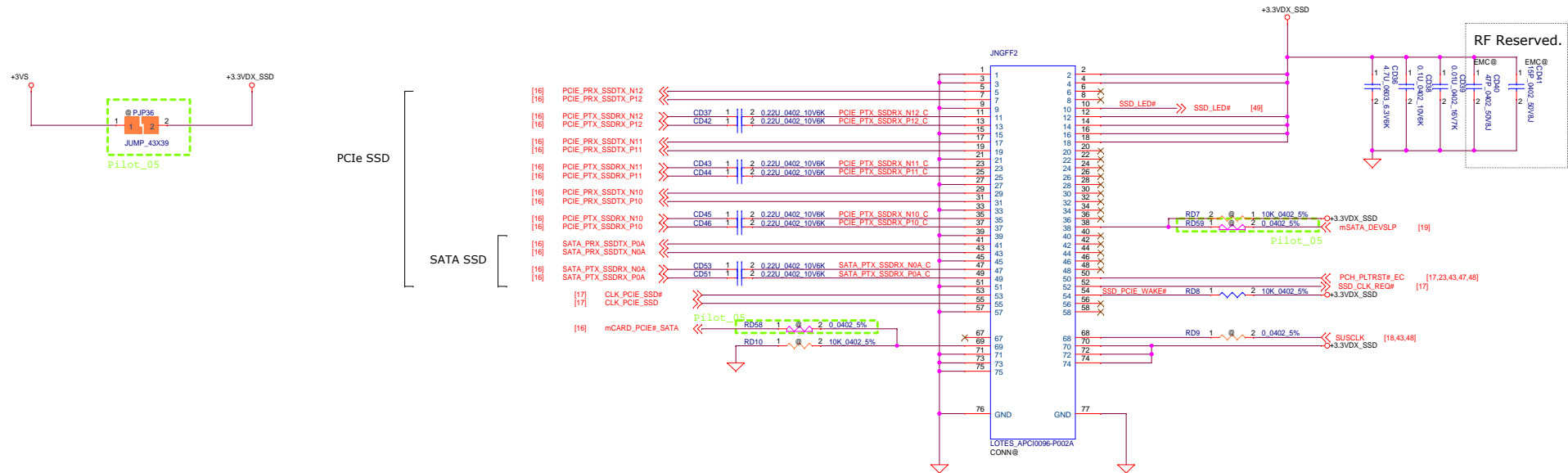
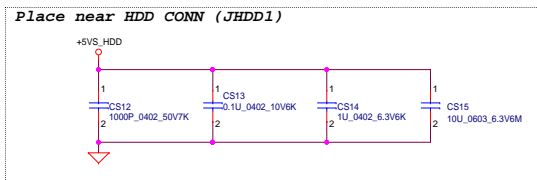
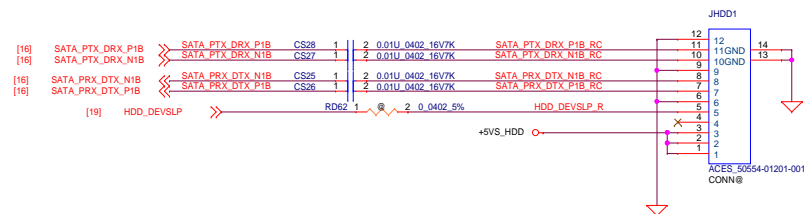
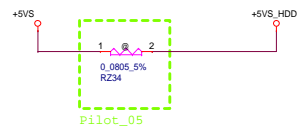


M.2 Slot-A Key-A (WLAN + BT)



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Size	C	Document Number	LA-D991P	Rev
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**M.2 Slot-C Key-M (SSD)**

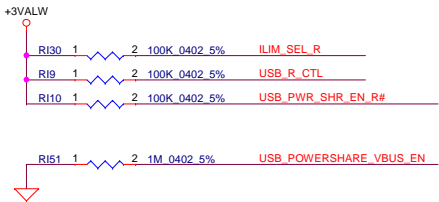
**HDD CONN**

Security Classification		Compal Secret Data		<div> <div>Compal Electronics, Inc.</div> <div>SSD</div> </div>	
Issued Date		Deciphered Date		Title	
2011/08/25		2012/07/25		<div> <div>Document Number</div> <div>LA-D991P</div> </div>	
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<div> <div>Date:</div> <div>Tuesday, November 08, 2016</div> </div>				<div> <div>Sheet</div> <div>44 of 70</div> </div>	

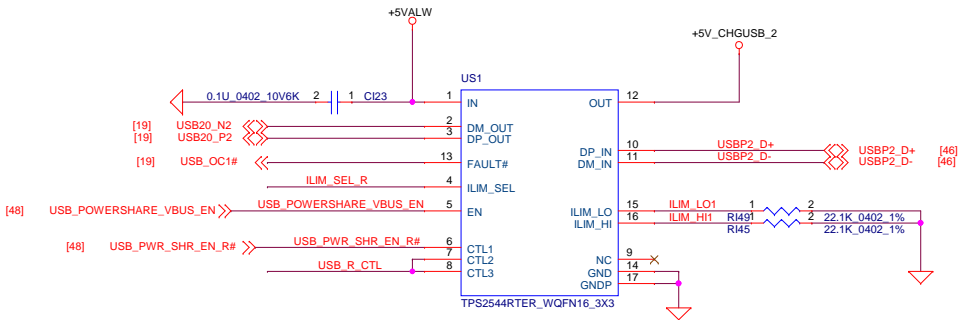
USB Powershare

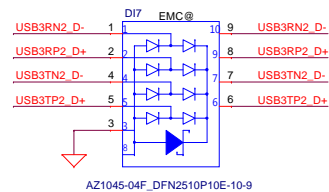
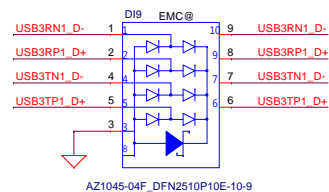
Device Control Pins				Flow Line Condition
CTL1	CTL2	CTL3	ILIM_SEL	
0	1	1	X	DCP AUTO
1	1	1	0	SDP
1	1	1	1	CDP

Suspend mode	CTL1 = 0 : Enable Power Share DCP mode in Suspend mode
	CTL1 = 1 : Disable Power Share in Suspend mode (For Support USB wake)
S0 mode	ILIM_SEL = 0 : SDP mode (0.9A by ILIM_LO setting)
	ILIM_SEL = 1 : CDP mode (STATUS# trigger by ILIM_HI =2.2A)

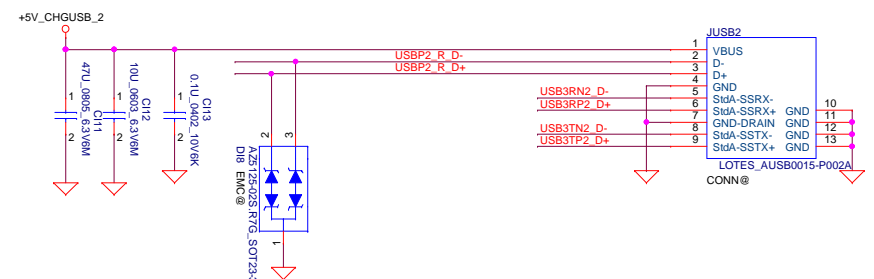


USB3.0 / USB2.0 Port1

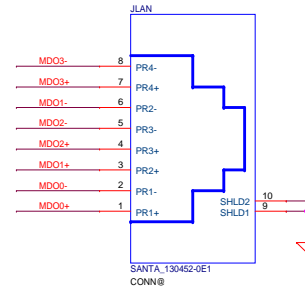
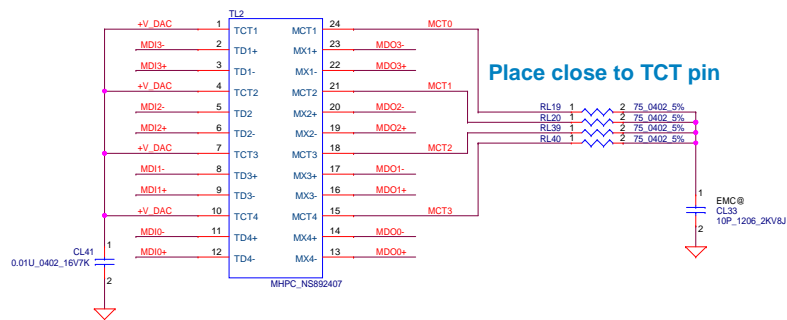
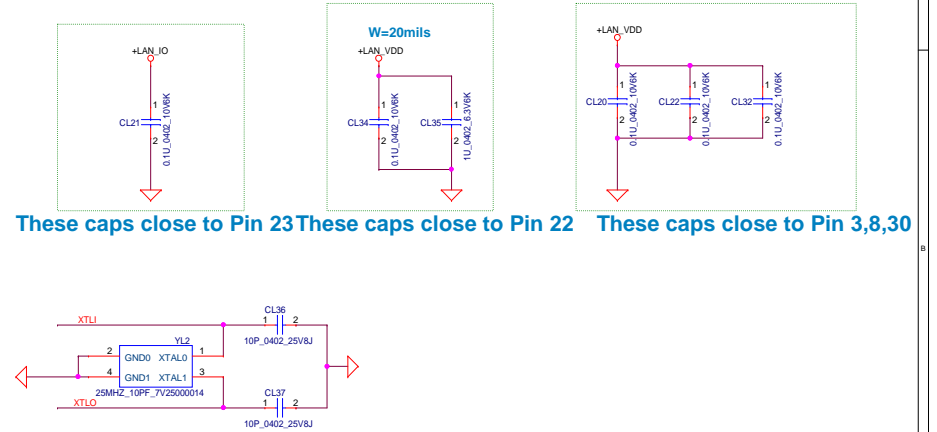
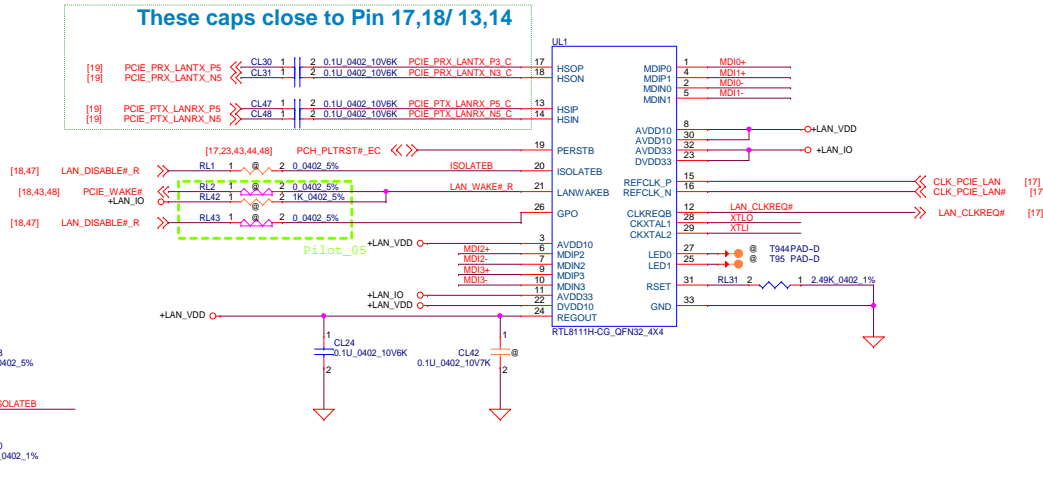
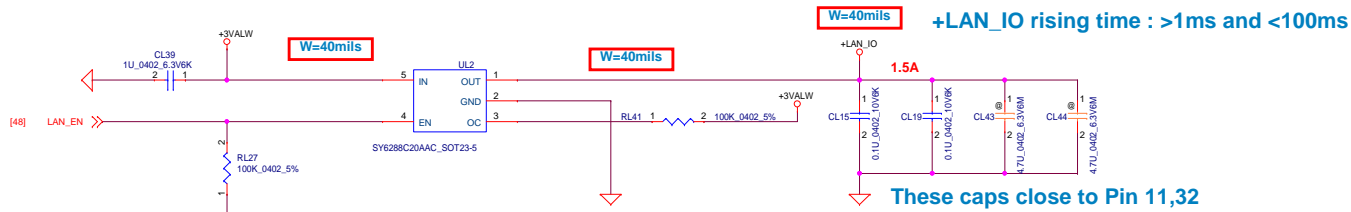


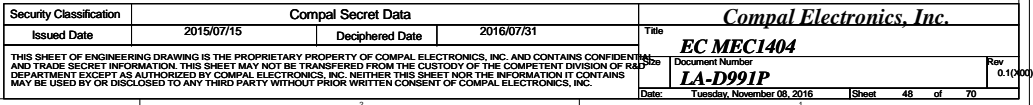


USB3.0 / USB2.0 Port2 (Power share)



Rev		
0.1(X100)		

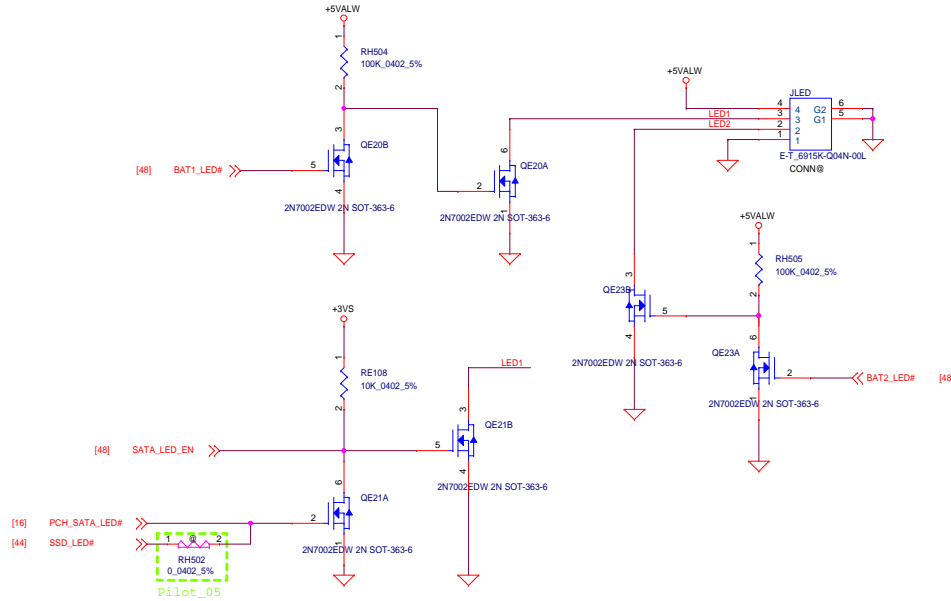




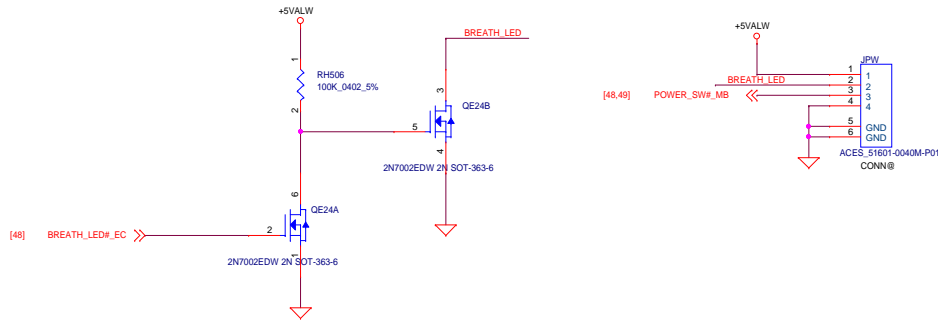


## LED Board Connector

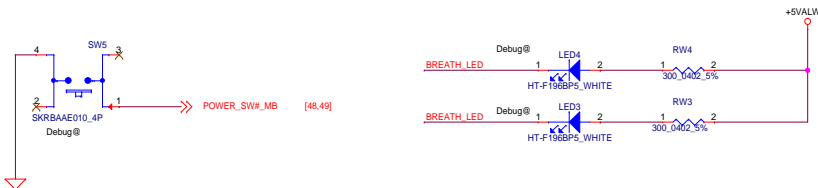
**+5VALW - Trace width : 20mil**



## TO PWR BOARD

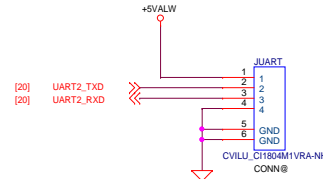


## Power Button & LED (Reserve)

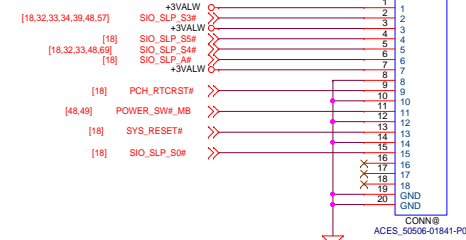


## I/O & APS & UART CONN

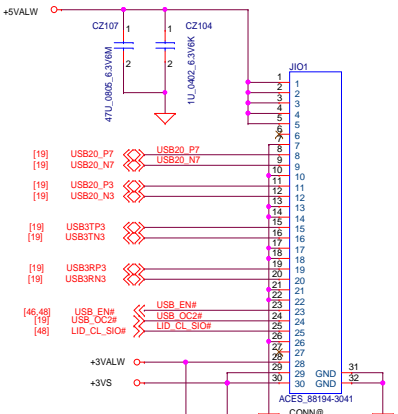
### UART CONN



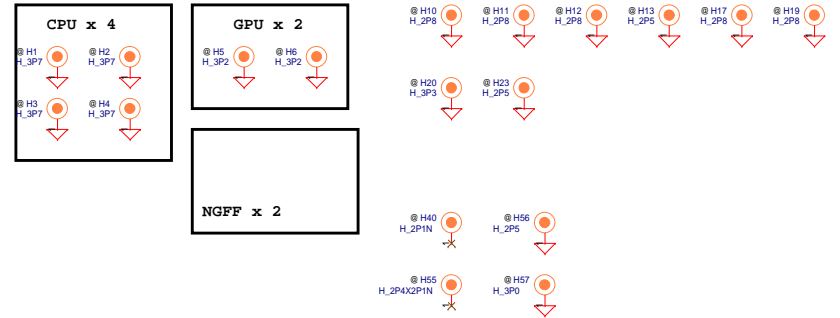
### APS CONN



### I/O CONN



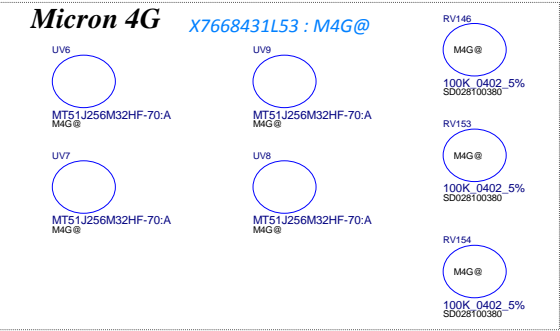
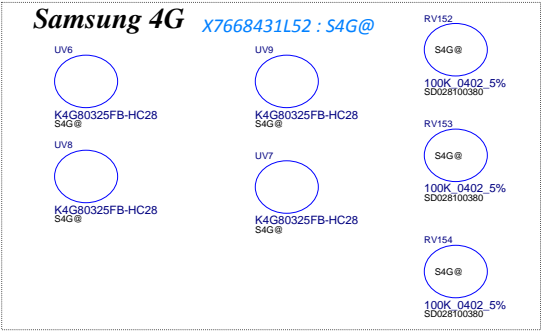
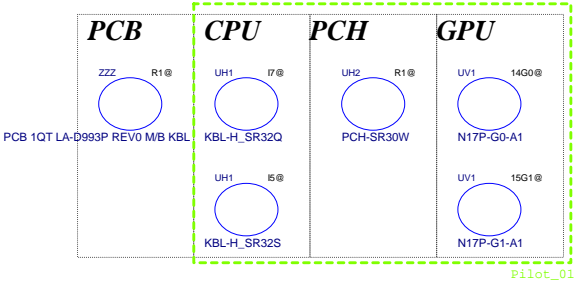
## Screw Hole



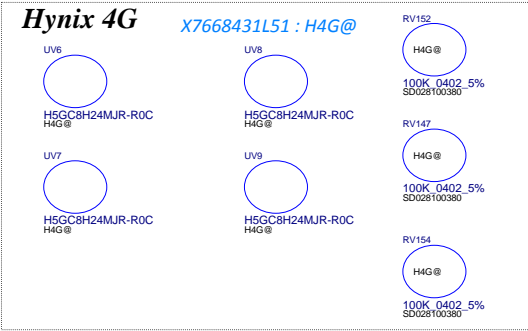
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Size	Document Number	Rev	0.1/200	
Date:	Tuesday, November 08, 2016	Sheet	49	of 70

MODEL NAME : *BBV00/ BBV10*  
PCB NO : *LA-D993P*

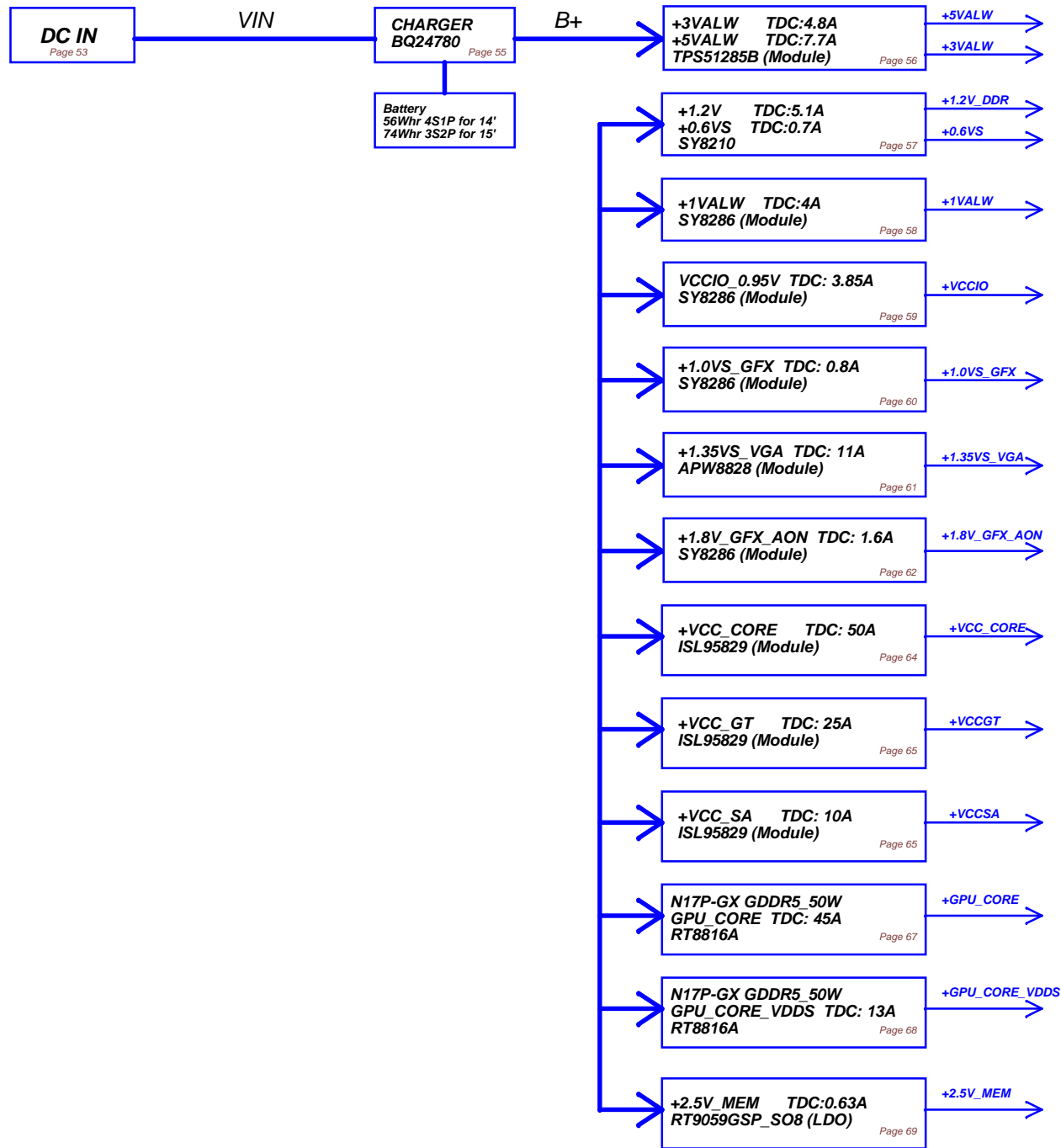
*Bom Structure*



*PRST*



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				LA-D993P	Rev 0.10000
				Date	Issued
				Tuesday, November 06, 2018	82 of 70



D



A

Rest of support elements (37.1)

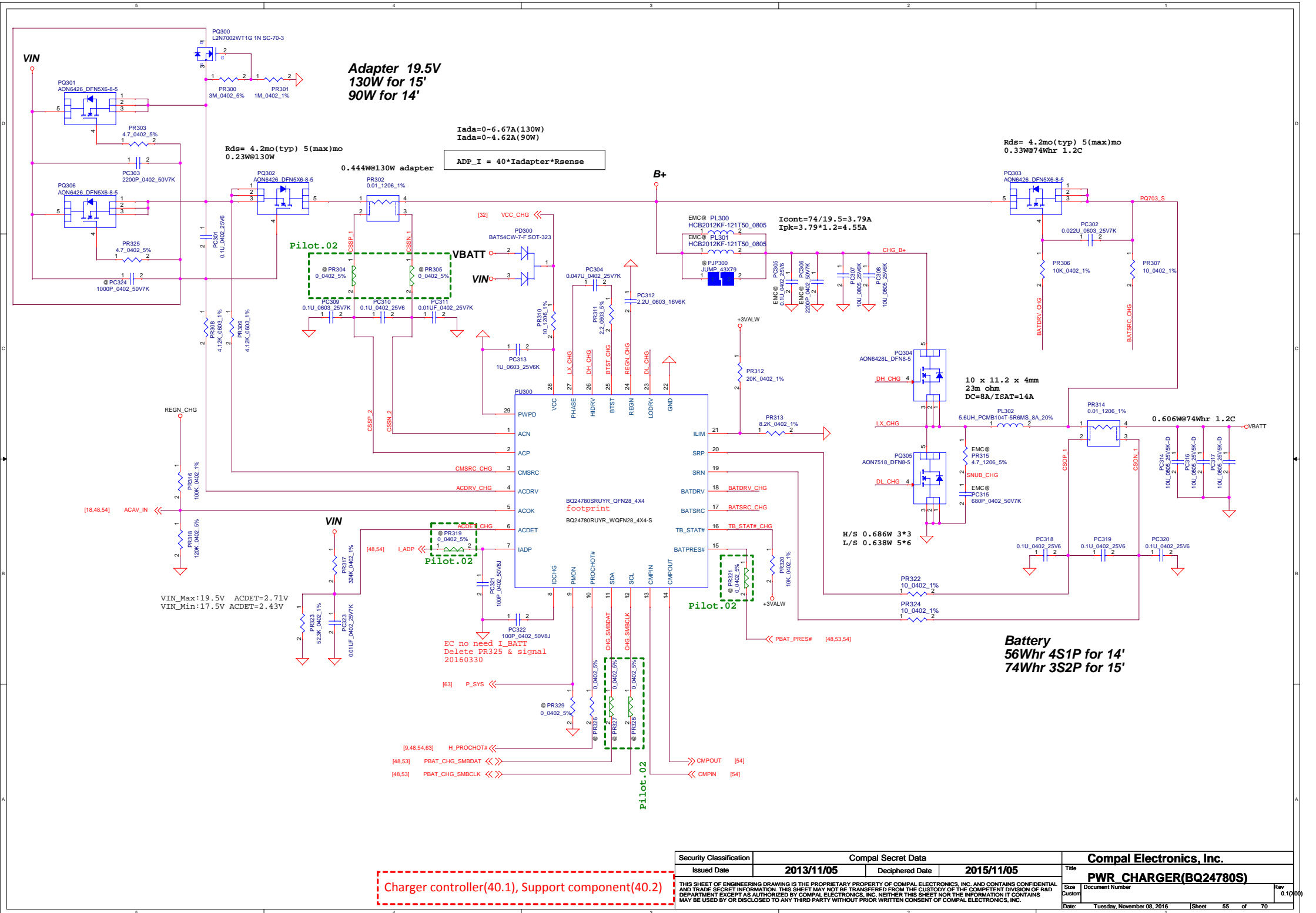


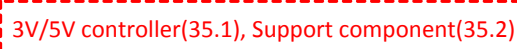
C



A

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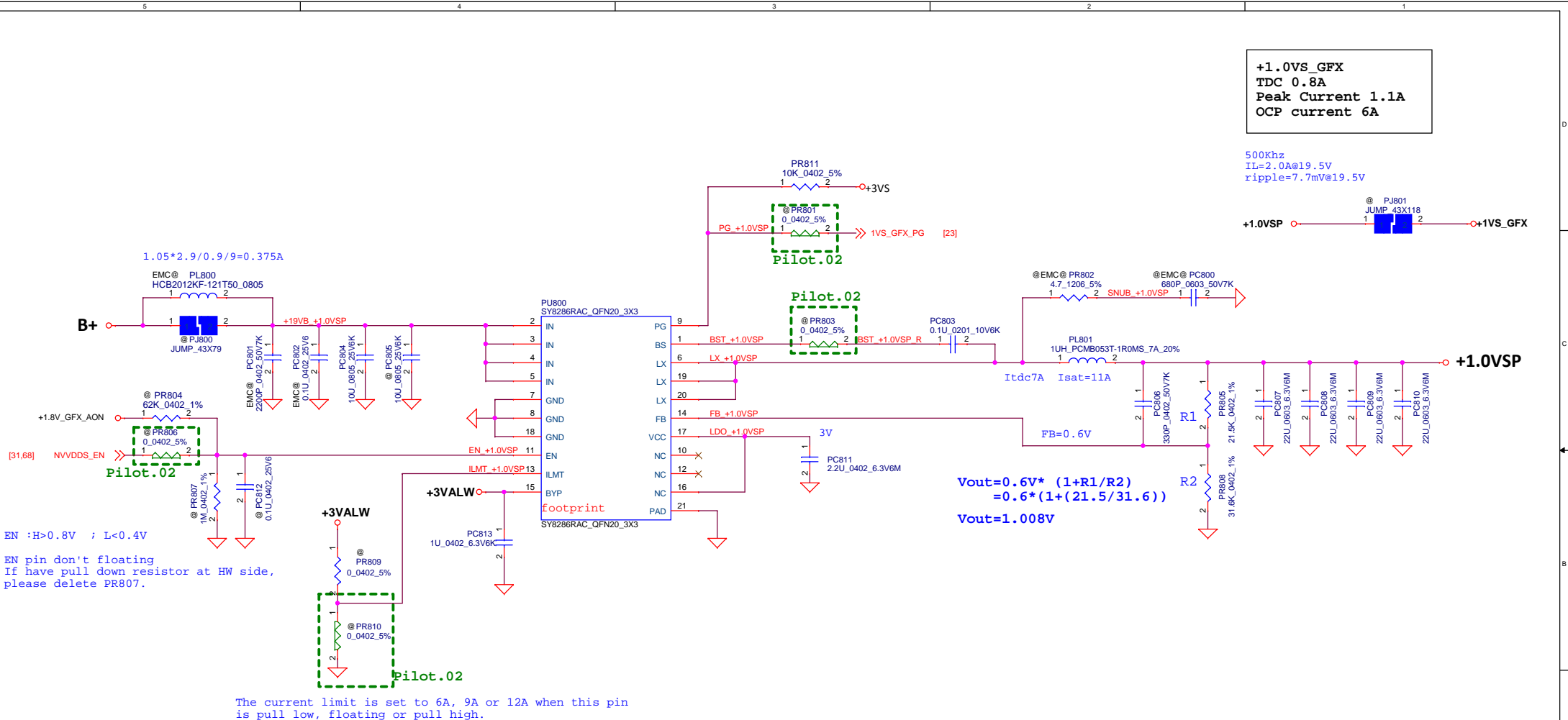
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2013/11/05	Deciphered Date	2015/11/05	Title	PWR 3.3VALWP/5VALWP	
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				Custom	LA-D993P	0.100
				Date: Tuesday, November 08, 2016		
				Sheet	56	of 70











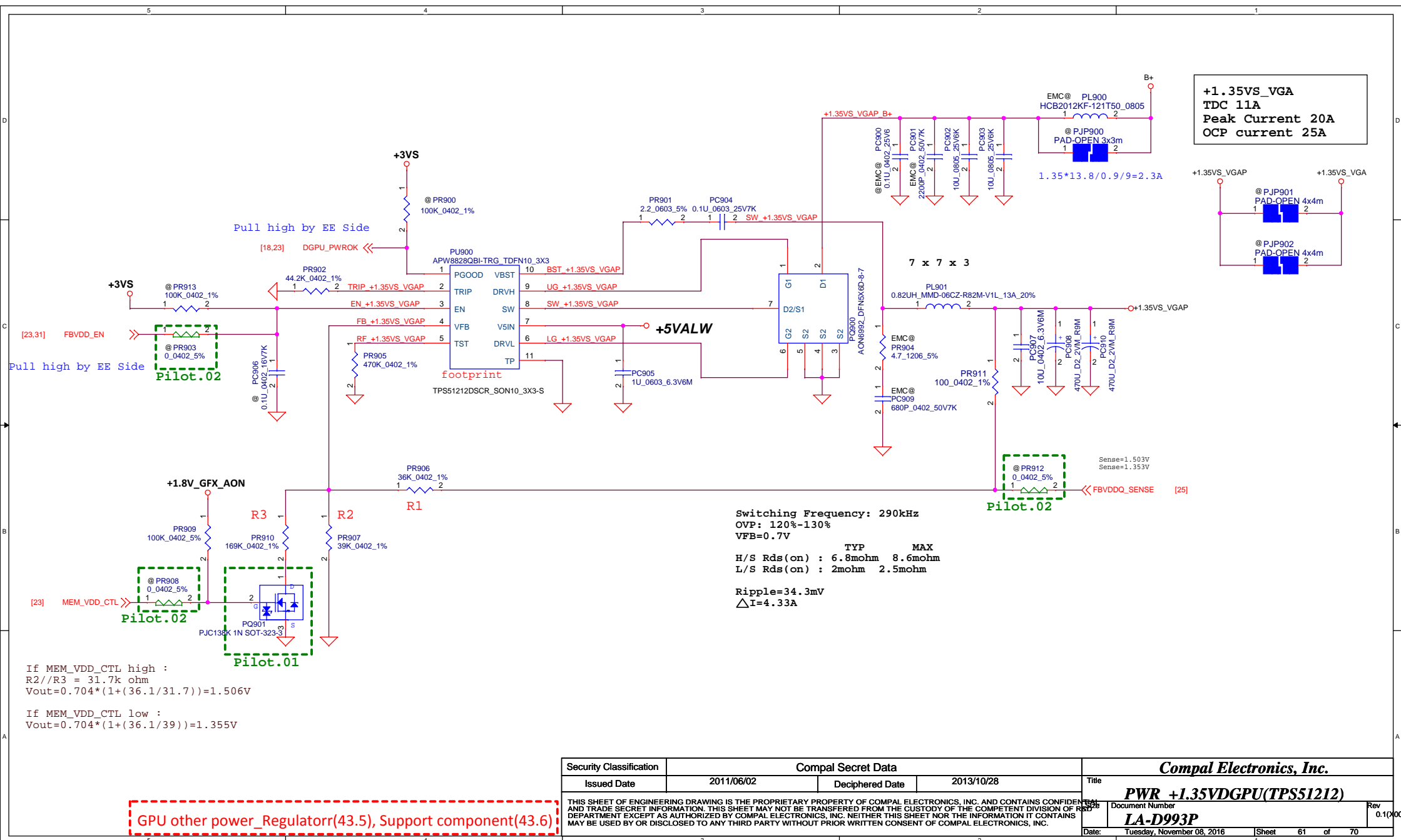
+1.0VS\_GFX  
TDC 0.8A  
Peak Current 1.1A  
OCP current 6A

500Khz  
IL=2.0A@19.5V  
ripple=7.7mV@19.5V

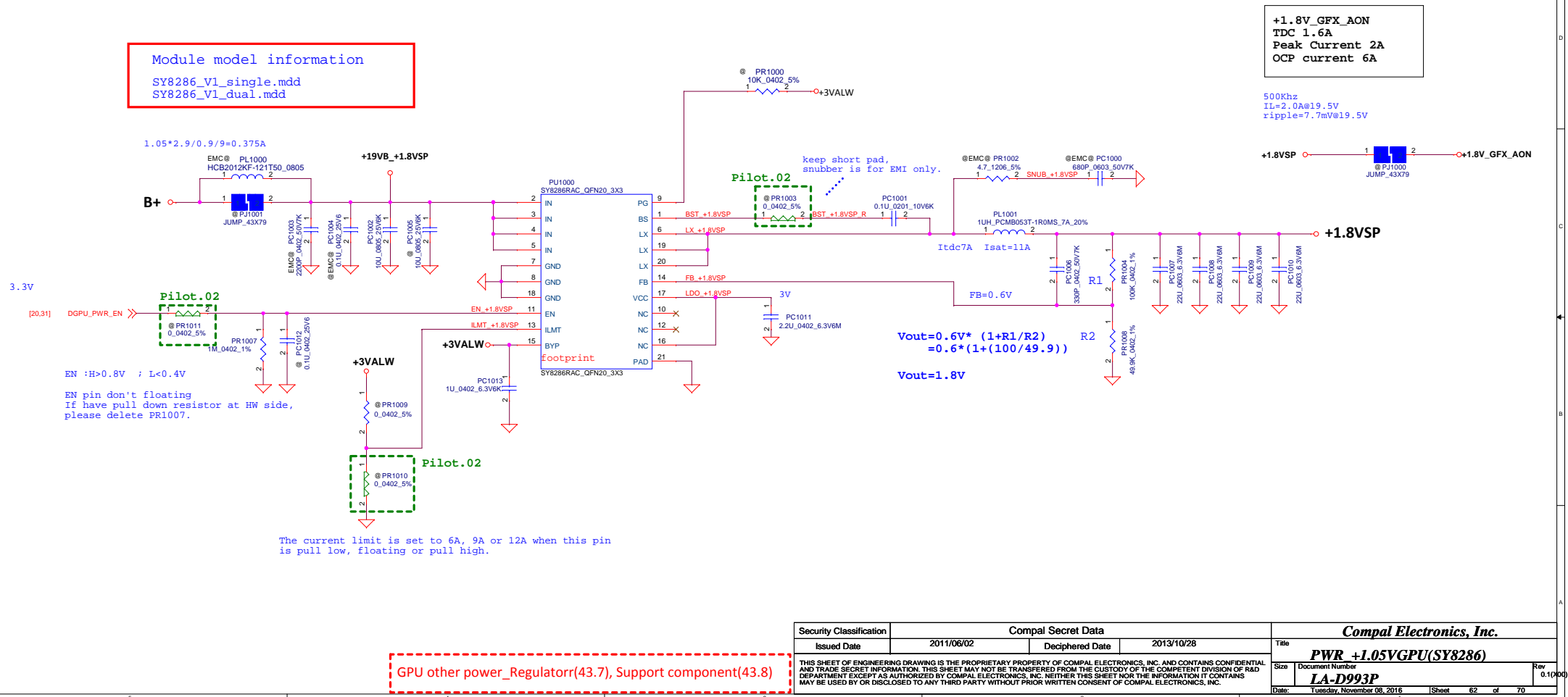
+1.0VSP → [PJ801 JUMP\_43X118] → +1VS\_GFX

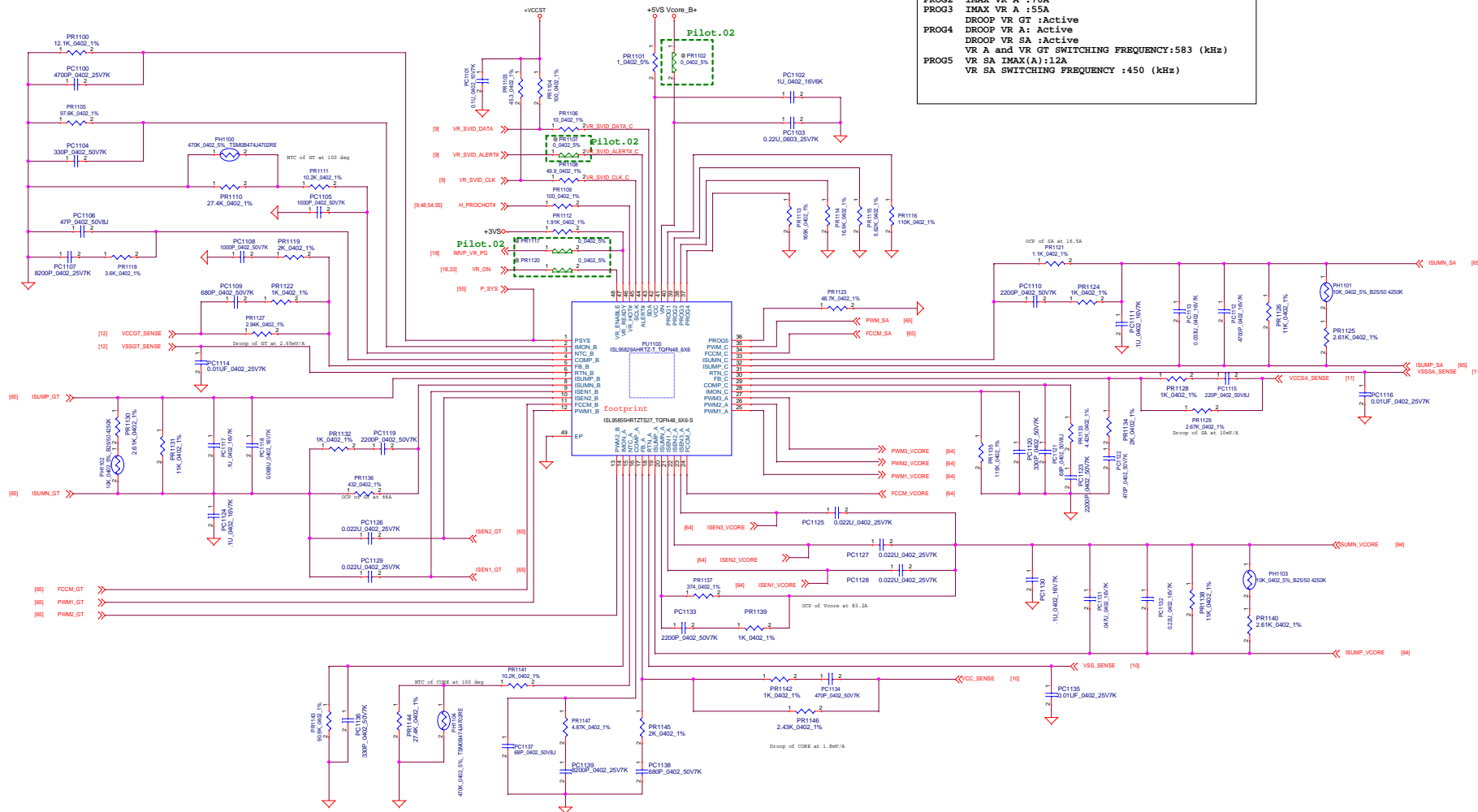
GPU other power\_Regulatorr(43.7), Support component(43.8)

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GPU other power\_Regulatorr(43.5), Support component(43.6)





PROG sets (Base on FMTBD.6 July 25, 2014)  
PROG1 Vboot :0V  
          slew rate :30 mV/us  
PROG2 IMAX VR A :70A  
PROG3 IMAX VR A :55A  
          DROOP VR GT :Active  
PROG4 DROOP VR A: Active  
          DROOP VR SA :Active  
          VR A and VR GT SWITCHING FREQUENCY:583 (kHz)  
PROG5 VR SA IMAX(A):12A  
          VR SA SWITCHING FREQUENCY :450 (kHz)

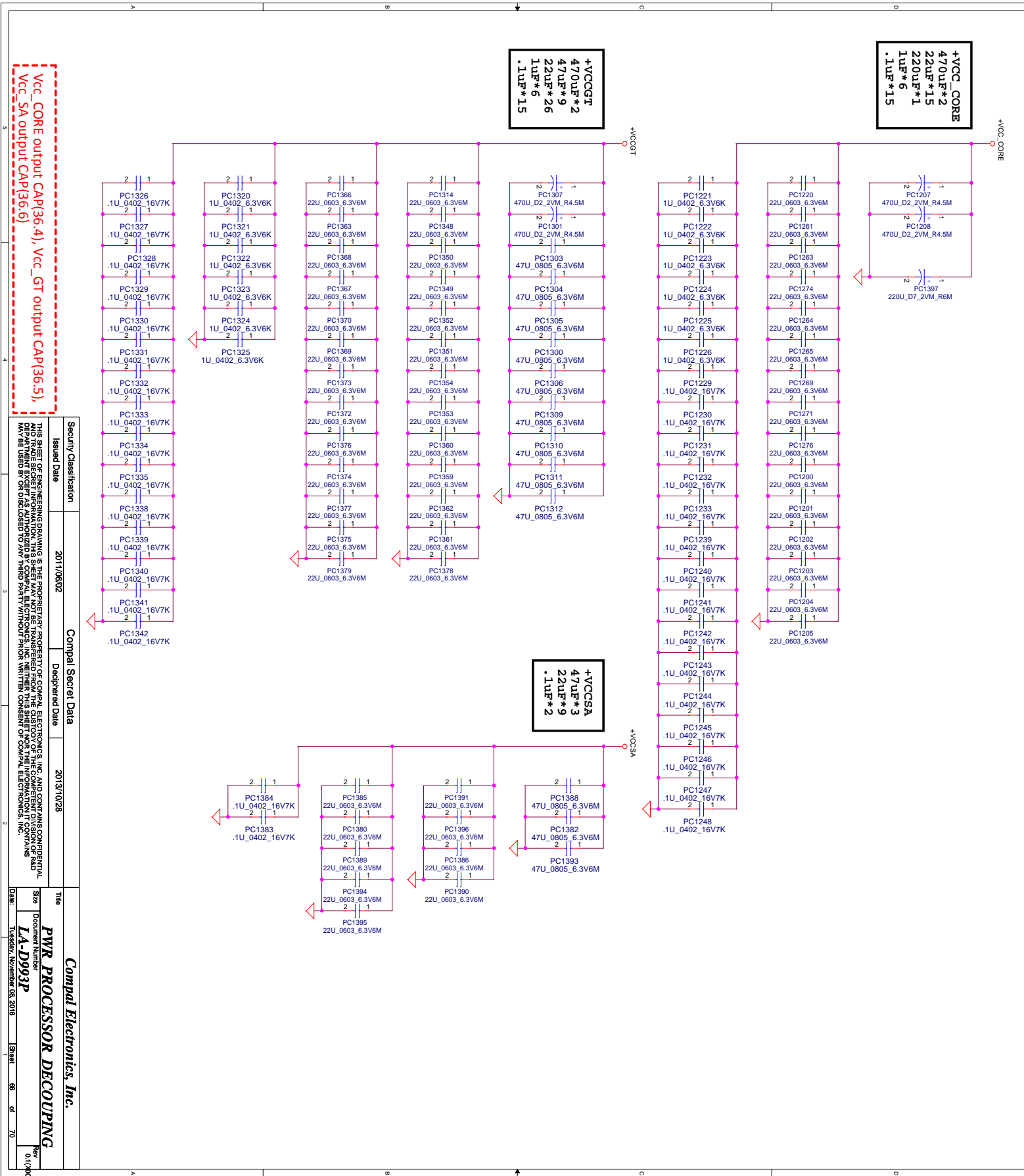
CPU\_Vcore controller(36.1),Drivers(36.2), Support component(36.3)  
Acoustic Noise B+ Bulk CAP(37.2)

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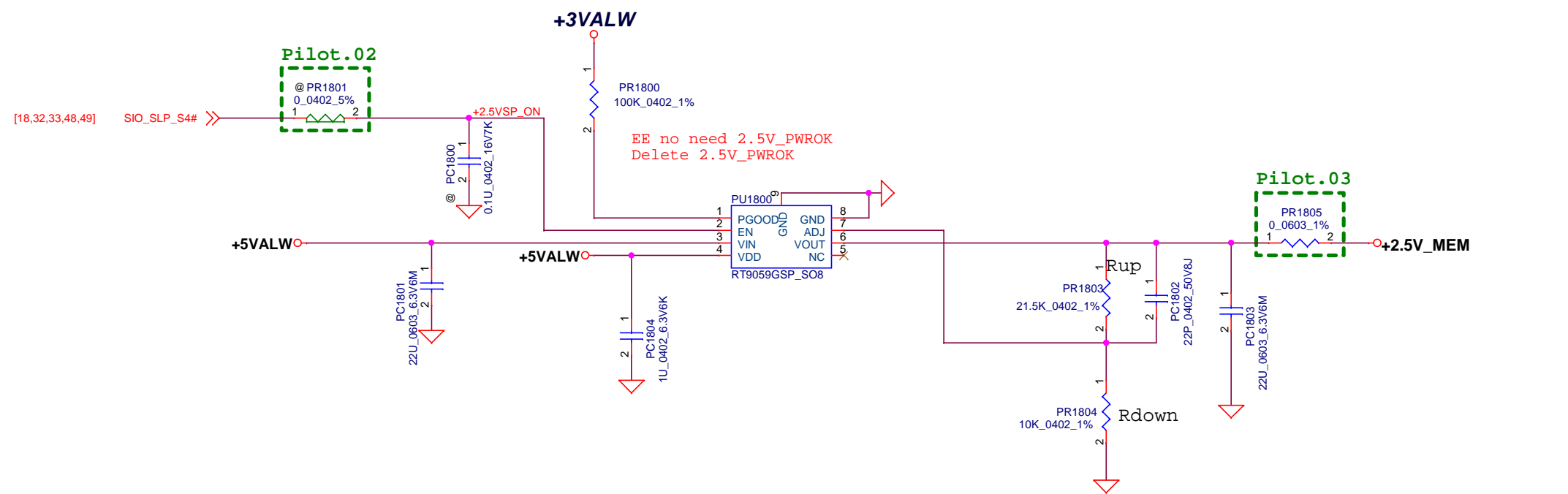






2.5V\_MEM controller(35.13), Support component(35.14)

+2.5V\_MEM  
TDC 0.63A  
Peak Current 0.9A  
OCP Current 3.5A



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